



# RS780CM-M5

V 1.0

08/212/'08

SCHEMATICS TABLE:

Page	Index	Page	Index
1	COVER PAGE	18	SB700-POWER & DECOUPLING
2	BLOCK DIAGRAM	19	SB700-SATA/IDE/HWM/SPI
3	HT,CPU MEMORY	20	SB700-STRAPS
4	CPU CONTROL & MISC	21	CRT(D-sub)-VGA
5	CPU PWR & GND	22	PCIE-16X/1X SLOT
6	DDR2 DIMM A CHANNEL	23	TPM, USB, 5VDUAL SWITCH
7	DDR2 DIMM B CHANNEL	24	PCI SLOT
8	DDR2 DIMM POWER	25	SIO IT8720,PS2,FDD,CIR
9	DDR2 DIMM TERMINATIONS	26	LPT/COM PORT
10	RS740/RS780-HT LINK I/F	27	LAN 8101E/8111C
11	RS740/RS780-PCIE I/F	28	AUDIO VIA1708B/ALC662
12	RS740/RS780-SYSTEM I/F	29	VIA1708B/ALC662(PANEL)
13	RS740/RS780-SPMEM/STRAPS	30	ISL6323 VCORE VOLTAGE
14	RS740/RS780-POWER	31	DC POWER, DDRII POWER
15	CLOCK GENERATOR-ICS9LPRS471	32	NB CORE POWER
16	SB700-PCIE/PCI/CPU/LPC/CLK	33	PANEL,ATX24P,SMRT FAN,BUZZER
17	SB700-ACPI/GPIO/USB/AUDIO	34	POWER ENABLE
		35	Attention

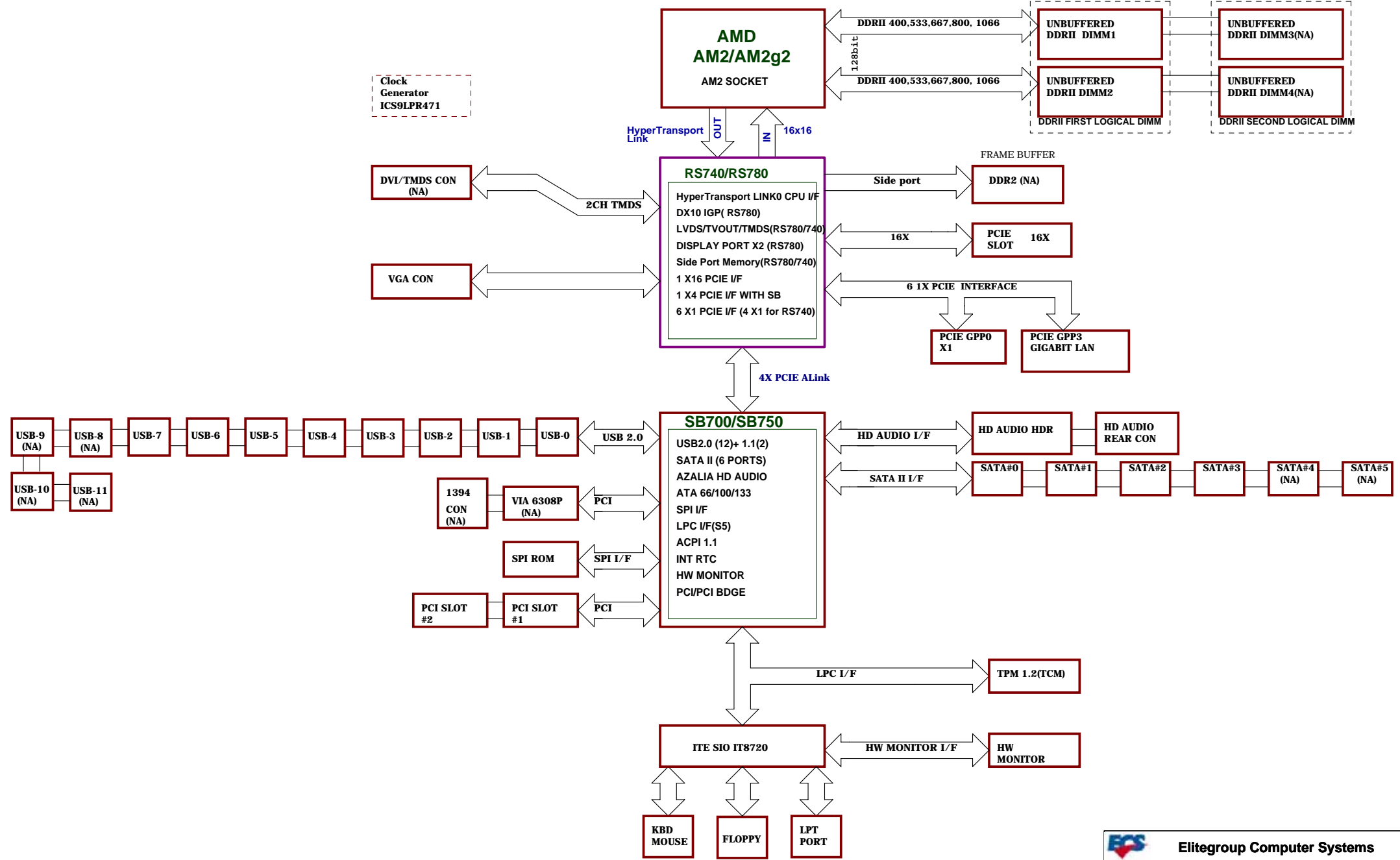
REVISION HISTORY:

Rev	Date	Notes
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PCB STACK: L1:TOP  
L2:PWR  
L3:GND  
L4:BOTTOM

# RS780CM-M5



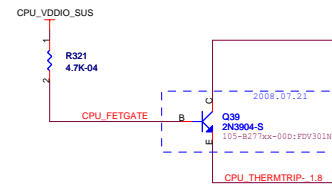
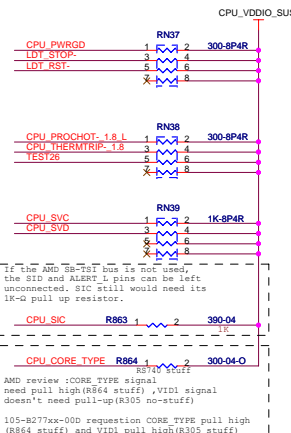
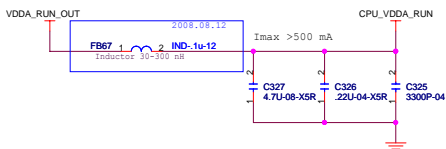
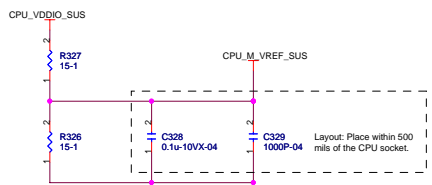
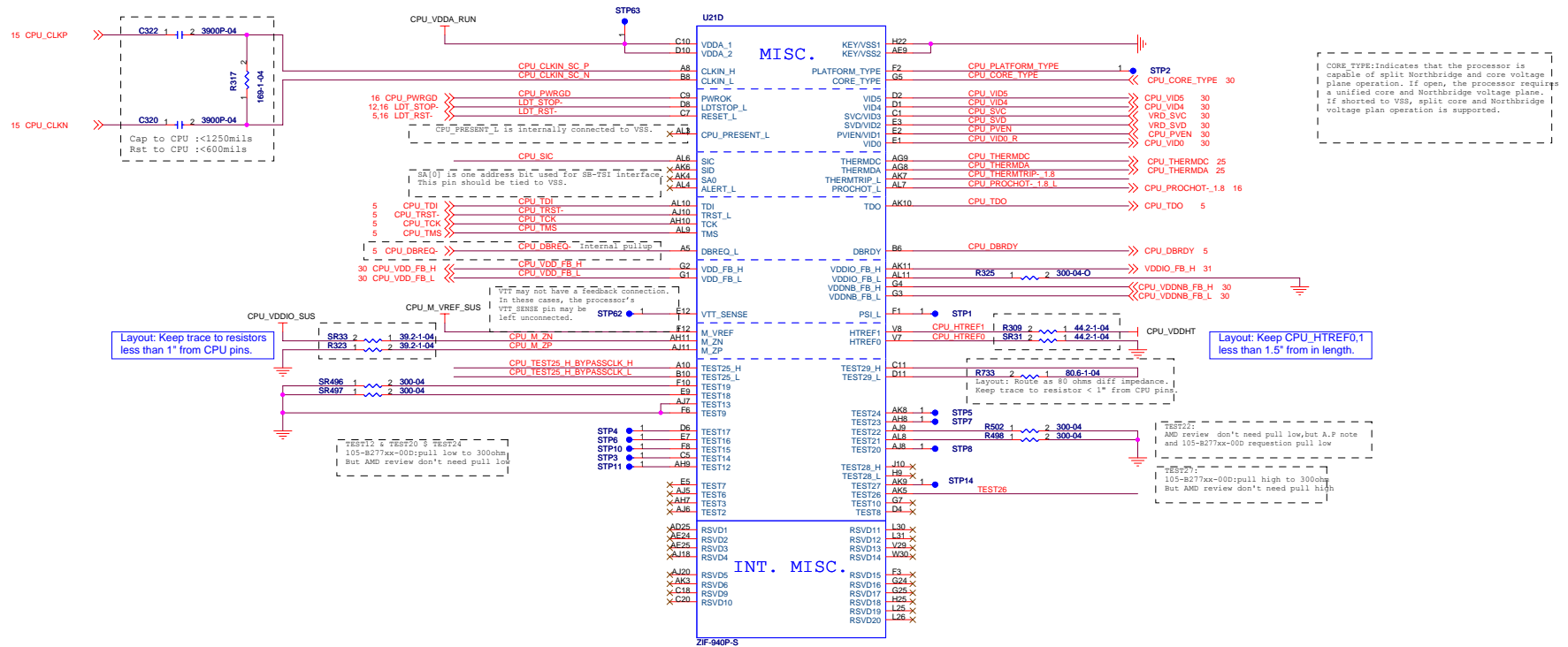
## HT LINK

## DDR2 Memory Interface B

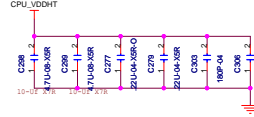
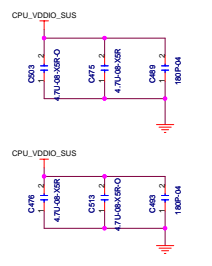
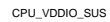
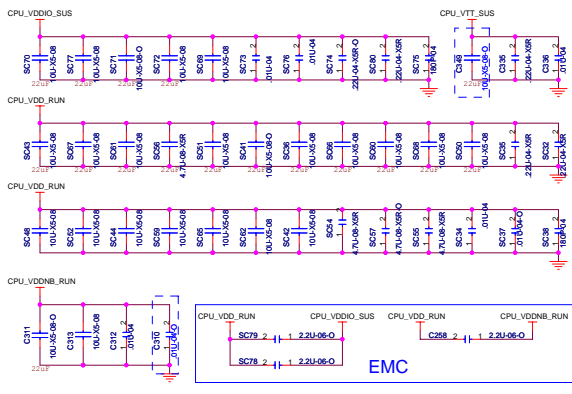
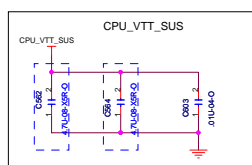
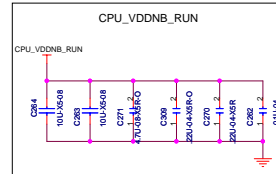
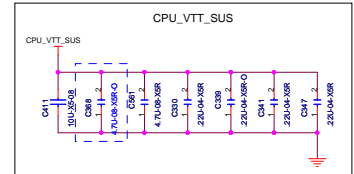
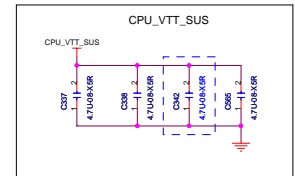
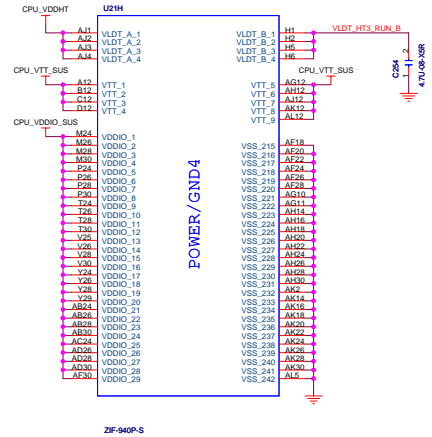
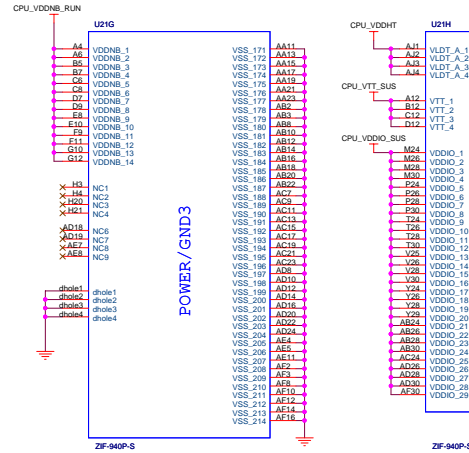
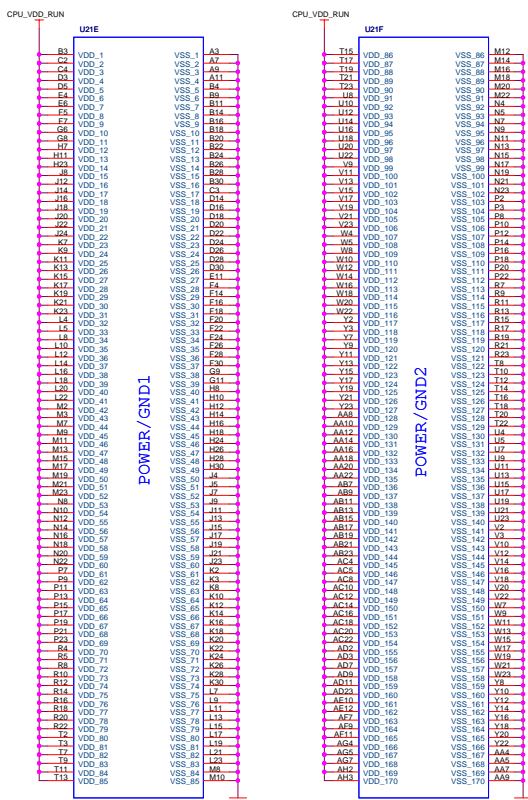


DIMM	DDR2 Memory Signal	CPU Signal
DIMM A0	MEM_MA0_CLK2	MA_CLK7
	MEM_MA0_CLK1	MA_CLK1
	MEM_MA0_CLK0	MA_CLK5
DIMM A1 (NA)	MEM_MA1_CLK2	MA_CLK6
	MEM_MA1_CLK1	MA_CLK0
	MEM_MA1_CLK0	MA_CLK4
DIMM B0	MEM_MB0_CLK2	MB_CLK7
	MEM_MB0_CLK1	MB_CLK1
	MEM_MB0_CLK0	MB_CLK5
DIMM B1 (NA)	MEM_MB1_CLK2	MB_CLK6
	MEM_MB1_CLK1	MB_CLK0
	MEM_MB1_CLK0	MB_CLK4

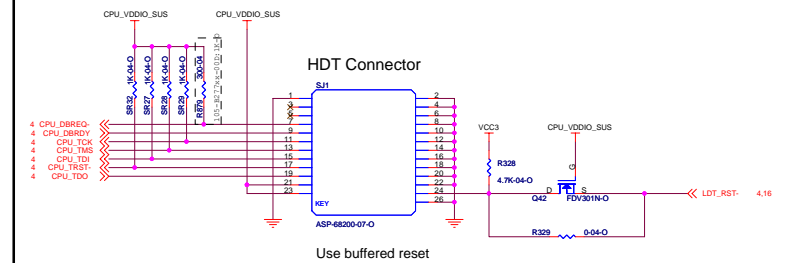
## CPU Control and Miscellaneous

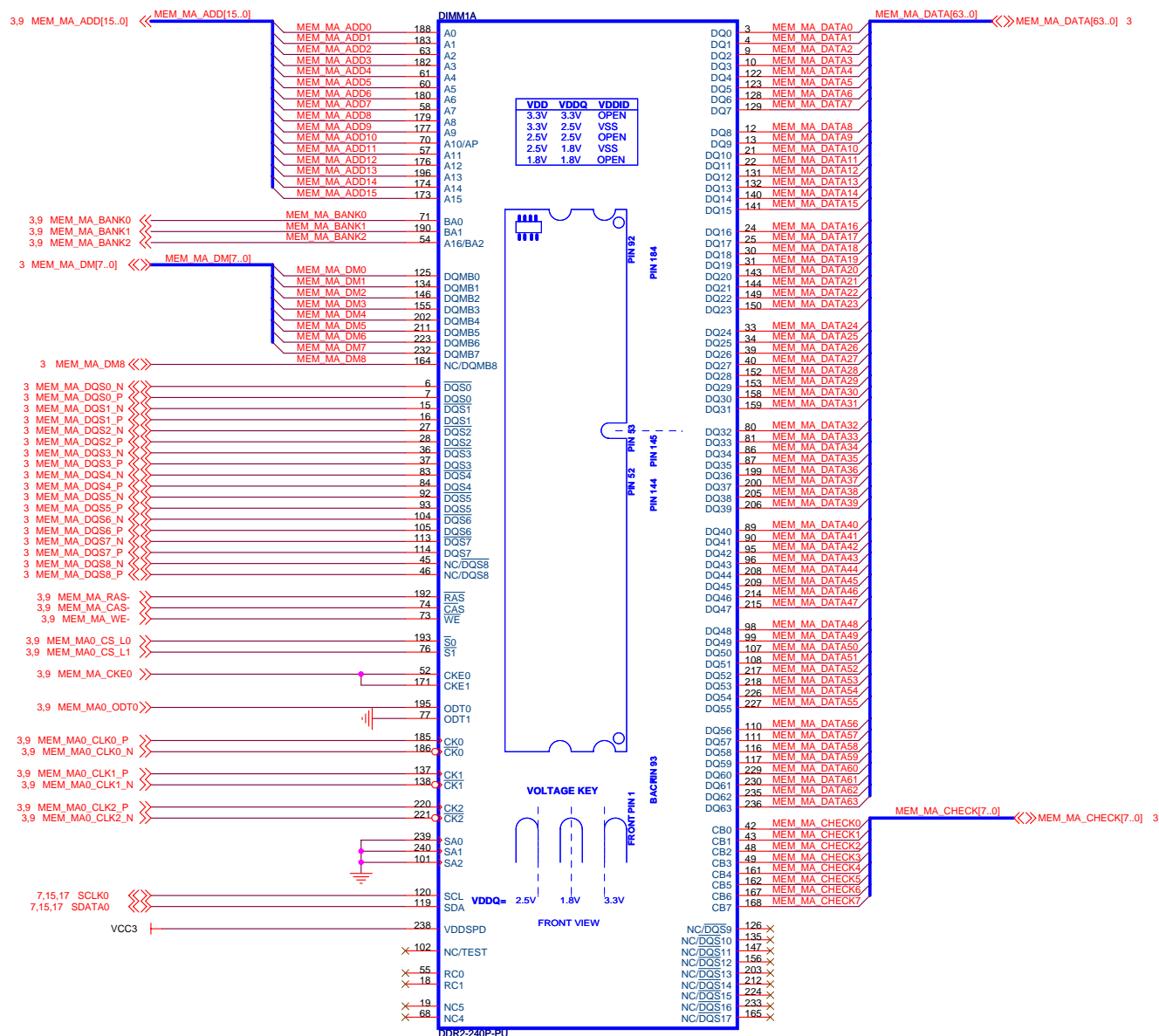


# Processor Power and Ground



## HDT Header

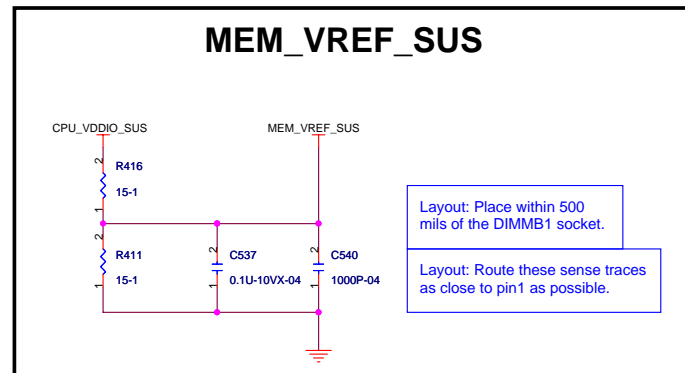
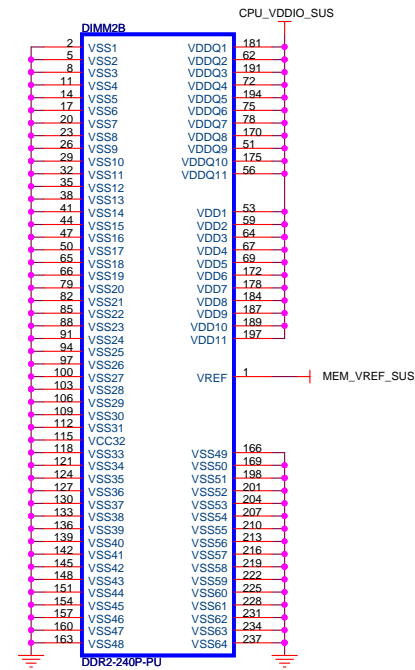
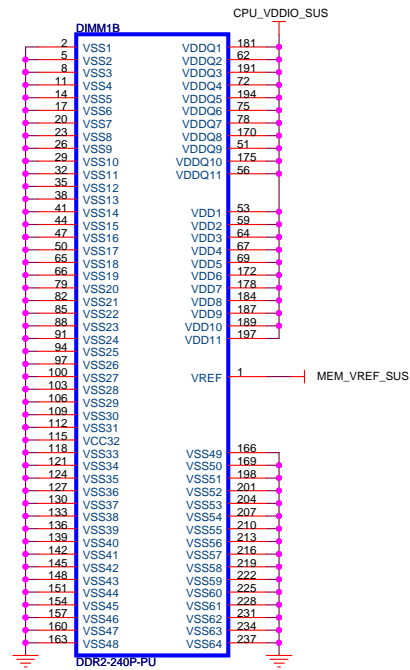


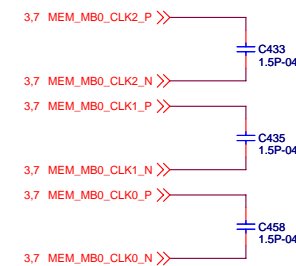
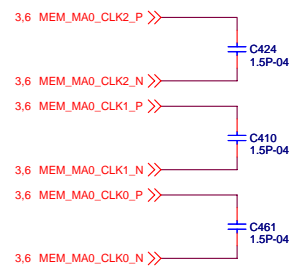
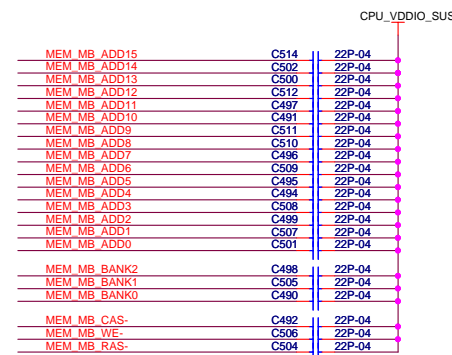
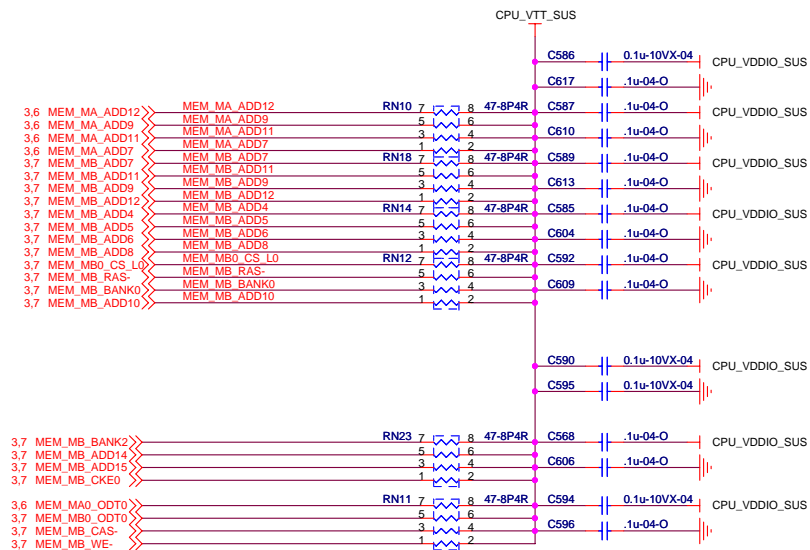



### SMBus Addressing

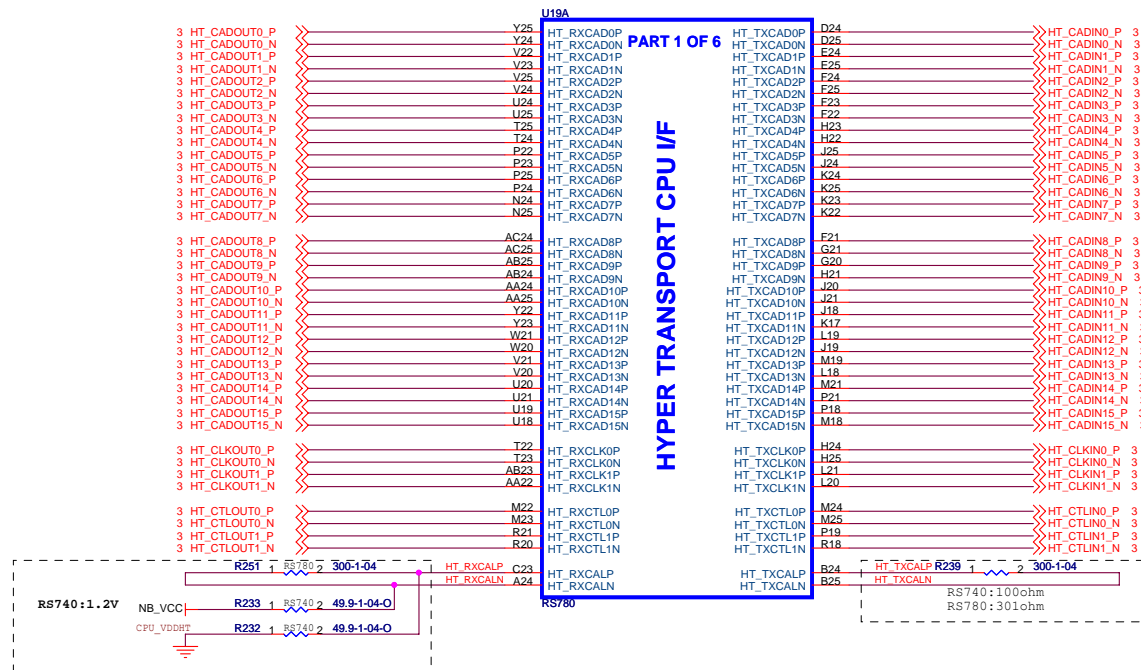
SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMB0	A2
DIMMA1	A4
DIMMB1	A6







 <b>Elitegroup Computer Systems</b>			
Title			
<b>DDR2 DIMM TERMINATIONS</b>			
Size	Document Number		Rev
Custom	<b>RS780CM-M5</b>		<b>1.0</b>
Date:	Wednesday, August 27, 2008	Sheet	9 of 35



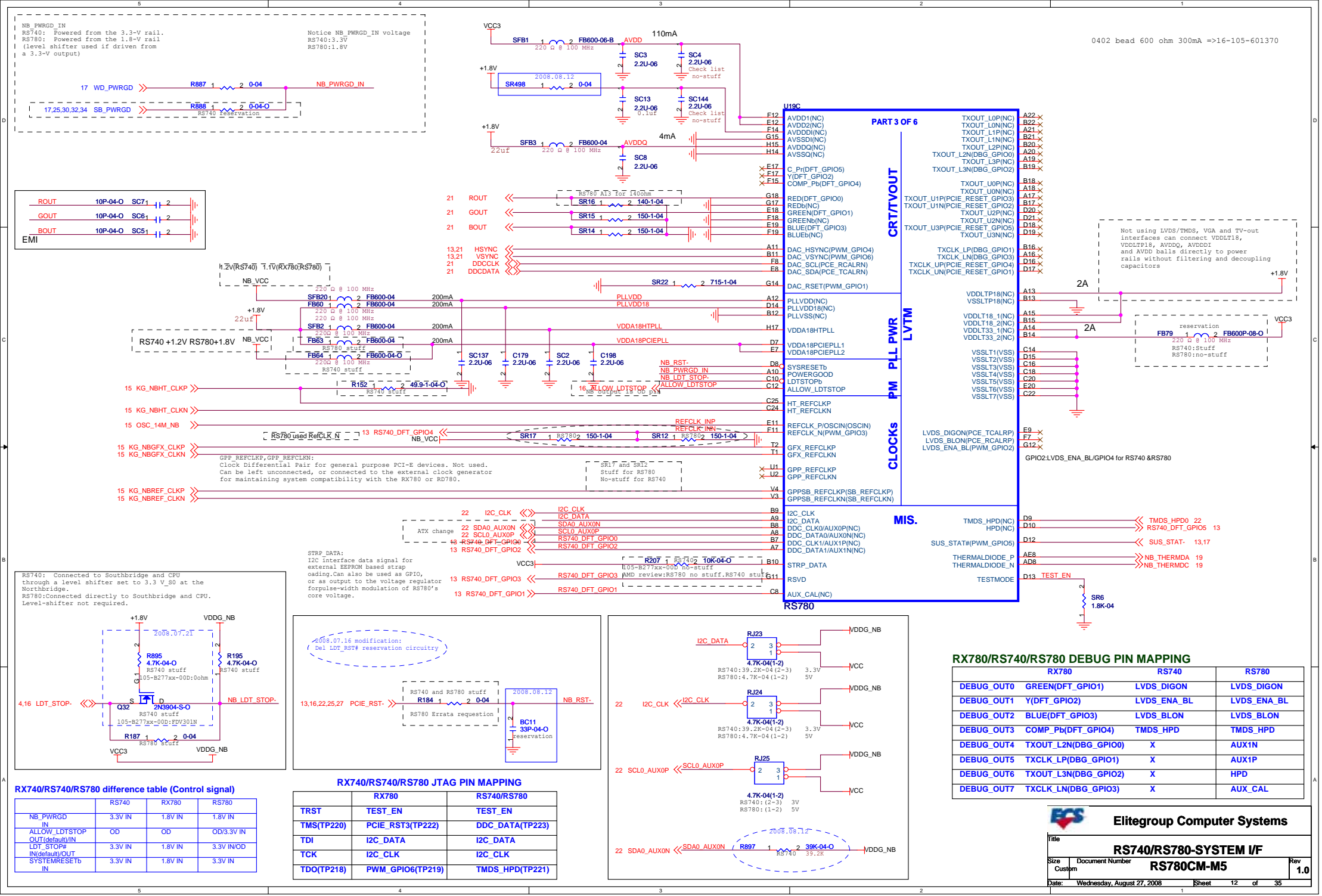
**RX780/RS740/RS780 difference table (HT LINK)**

SIGNALS	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP	100R	1.21K	301R
HT_TXCALN			



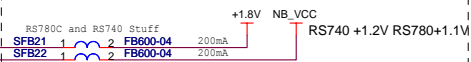
**Elitegroup Computer Systems**





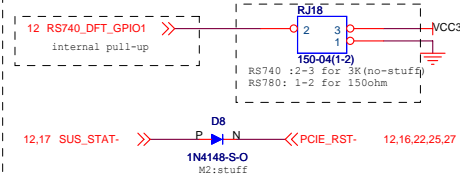
U19D			
PAR 4 OF 6			
AB12	MEM_A0(NC)	MEM_DQ0/DVO_VSYNC(NC)	AA18
AE16	MEM_A1(NC)	MEM_DQ1/DVO_HSYNC(NC)	AA20
V11	MEM_A2(NC)	MEM_DQ2/DVO_DE(NC)	AA19
AE15	MEM_A3(NC)	MEM_DQ3/DVO_DQ(NC)	Y19
AA12	MEM_A4(NC)	MEM_DQ4(NC)	Y17
AB16	MEM_A5(NC)	MEM_DQ5/DVO_D1(NC)	AA17
AB14	MEM_A6(NC)	MEM_DQ6/DVO_D2(NC)	AA15
AD14	MEM_A7(NC)	MEM_DQ7/DVO_D4(NC)	AC29
AD13	MEM_A8(NC)	MEM_DQ8/DVO_D3(NC)	AD19
AC16	MEM_A9(NC)	MEM_DQ9/DVO_D5(NC)	AE22
AE13	MEM_A10(NC)	MEM_DQ10/DVO_D6(NC)	AC14
AC14	MEM_A11(NC)	MEM_DQ11/DVO_D7(NC)	AB20
X Y14	MEM_A12(NC)	MEM_DQ12(NC)	AD22
	MEM_A13(NG)	MEM_DQ13/DVO_D8(NC)	AC22
		MEM_DQ14/DVO_D10(NG)	AD21
AD15	MEM_BA0(NC)	MEM_DQ15/DVO_D11(NG)	
AE17	MEM_BA1(NC)		Y17
AD17	MEM_BA2(NG)	MEM_DQS0P/DVO_IDCKP(NG)	W18
		MEM_DQS0N/DVO_IDCKP(NG)	AD29
X W12	MEM_RASb(NG)	MEM_DQS1P(NG)	AE2
X Y12	MEM_CASb(NG)	MEM_DQS1N(NG)	
AD18	MEM_WEb(NG)		W17
AB13	MEM_CSb(NG)	MEM_DM0(NG)	AE19
AB18	MEM_CKE(NG)	MEM_DM1/DVO_D8(NG)	
X Y14	MEM_ODT(NG)		
		IOPLLVD18(NG)	AE23
X V15	MEM_CKP(NG)	IOPLLVD(NG)	AE24
W14	MEM_CKN(NG)		
		IOPLLVS(NG)	AD23
AE12	MEM_COMP(NG)		
AD12	MEM_COMPN(NG)	MEM_VREF(NG)	AE18

Note: For the RS780C, which does not support a side-port memory interface, these balls should still be connected to an isolated 1.1V(1.8V) power rail.



## RS740/RX780/RS780 STRAPS

Note: for RS780, change RJ18 to 150R as AUX\_CAL, place close to pin C8



### RS740/RX780/RS780: LOAD\_EEPROM\_STRAPS

Selects Loading of STRAPS from EPROM

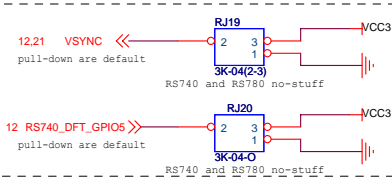
1 : Bypass the loading of EEPROM straps and use Hardware Default Values

0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS740: pin DFT\_GPIO1

RX780: pin DFT\_GPIO1

RS780: pin SUS\_STAT#



### RS740/RX780/RS780: STRAP\_DEBUG\_BUS\_GPIO\_ENABLE

Enables the Test Debug Bus using GPIO and/or memory IO

1 : Disable (RS740/RS780); Enable (RX780)

0 : Enable (RS740/RS780); Disable (RX780)

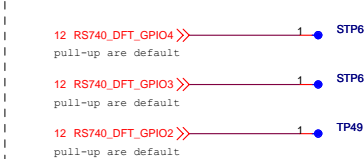
RS740: pin DFT\_GPIO5

RX780: pin DFT\_GPIO5

RS780: pin VSYNC

### RS780: STRAP\_PCIE\_GPP\_CFG[2:0] (configure thru register setting)

1-1-1-1-1-1	Mode L	default
1-1-1-1-1-1	Mode L	
2-0-2-0-2-0	Mode C2	
2-0-2-0-1-1	Mode K	
2-0-1-1-1-1	Mode E	
1-1-1-1-1-1	Mode L	
4-0-0-0-1-1	Mode C	
4-0-0-0-2-0	Mode B	



### RS740: STRAP\_PCIE\_SB/GPP\_CFG[2:0] (Pins: RS740\_DFT\_GPIO[4:2])

These pin straps are used to configure PCI-E GPP mode.

111: register defined (register default to Config E) default

110: 4-0-0-0-0 Config A

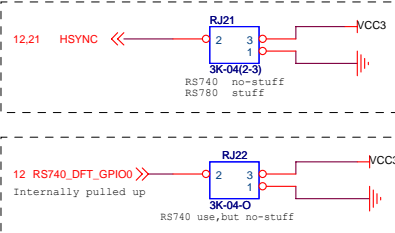
101: 4-4-0-0-0 Config B

100: 4-2-2-0-0 Config C

011: 4-2-1-1-0 Config D

010: 4-1-1-1-1 Config E

others: register defined (default to Config E)



### RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE

Enables Side port memory

1. Disable (RS740/RS780)

0 : Enable (RS740/RS780)

RS740: pin DFT\_GPIO0

RS780: pin HSYNC

RX780: Not Applicable

### RX780/RS780: STRAP\_DEBUG\_BUS\_PCIE\_ENABLE

Enables Test debug bus using PCIE bus

1. Disable (can be enabled thru nbcfg register)

0 : Enable

RX780: pin DFT\_GPIO0

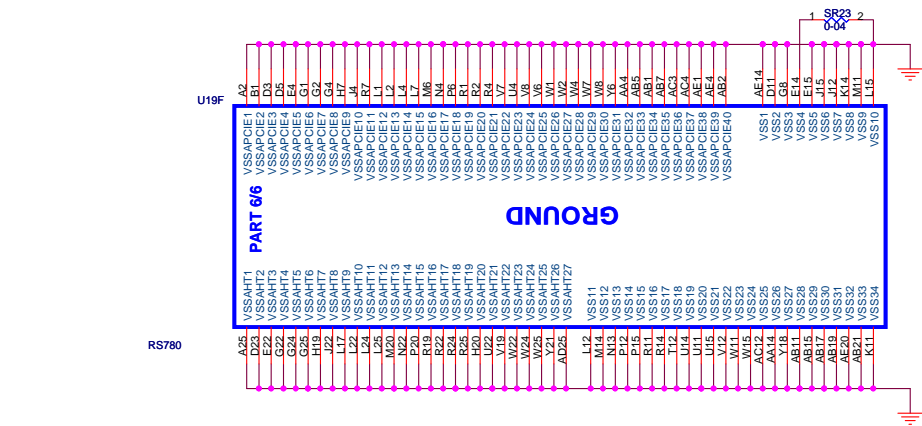
RS780: configurable thru register setting only

RS740: Not supported



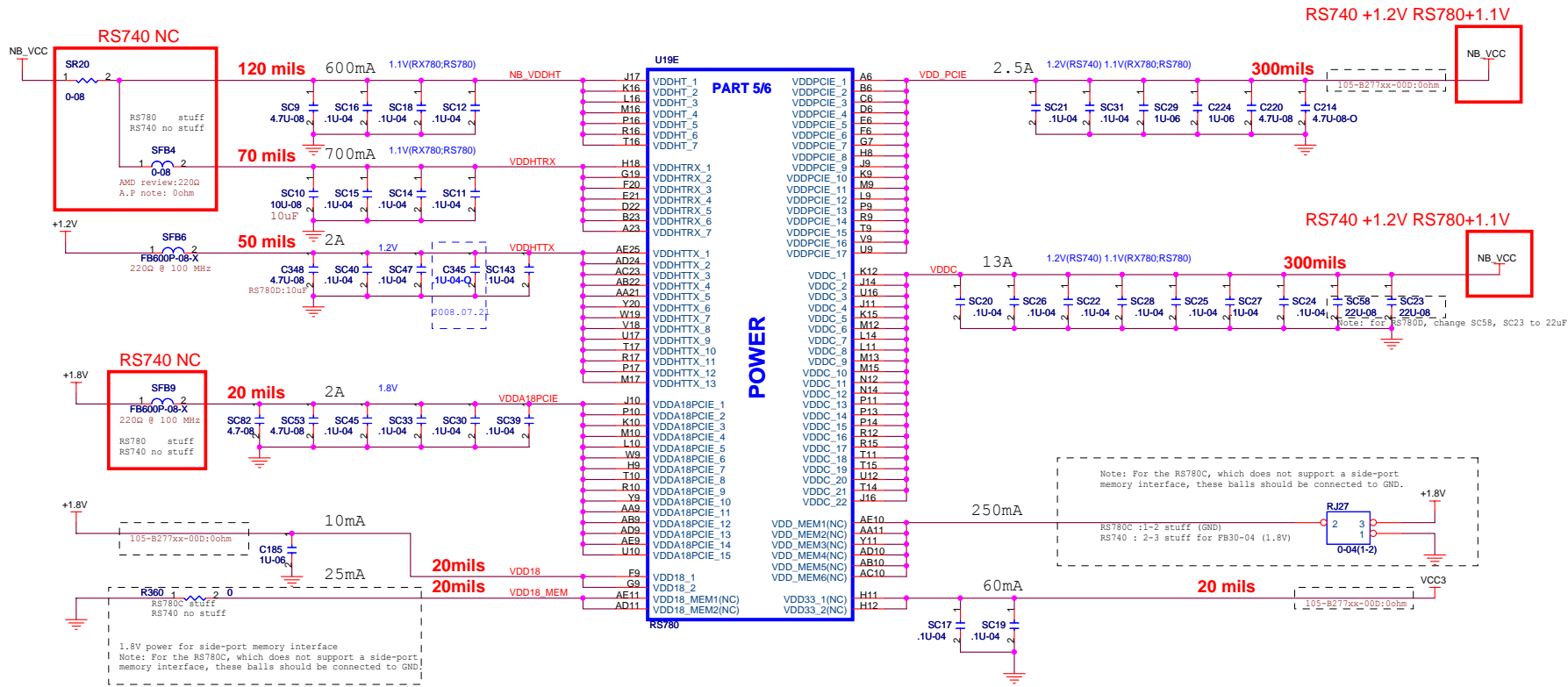
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Title	RS740/RS780-SPMEM/STRAPS		
Size	Document Number	RS780CM-M5	Rev 1.0
Date:	Wednesday, August 27, 2008	Sheet 13	of 35



RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLTP18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDLTP18	+1.8V	NC	+1.8V

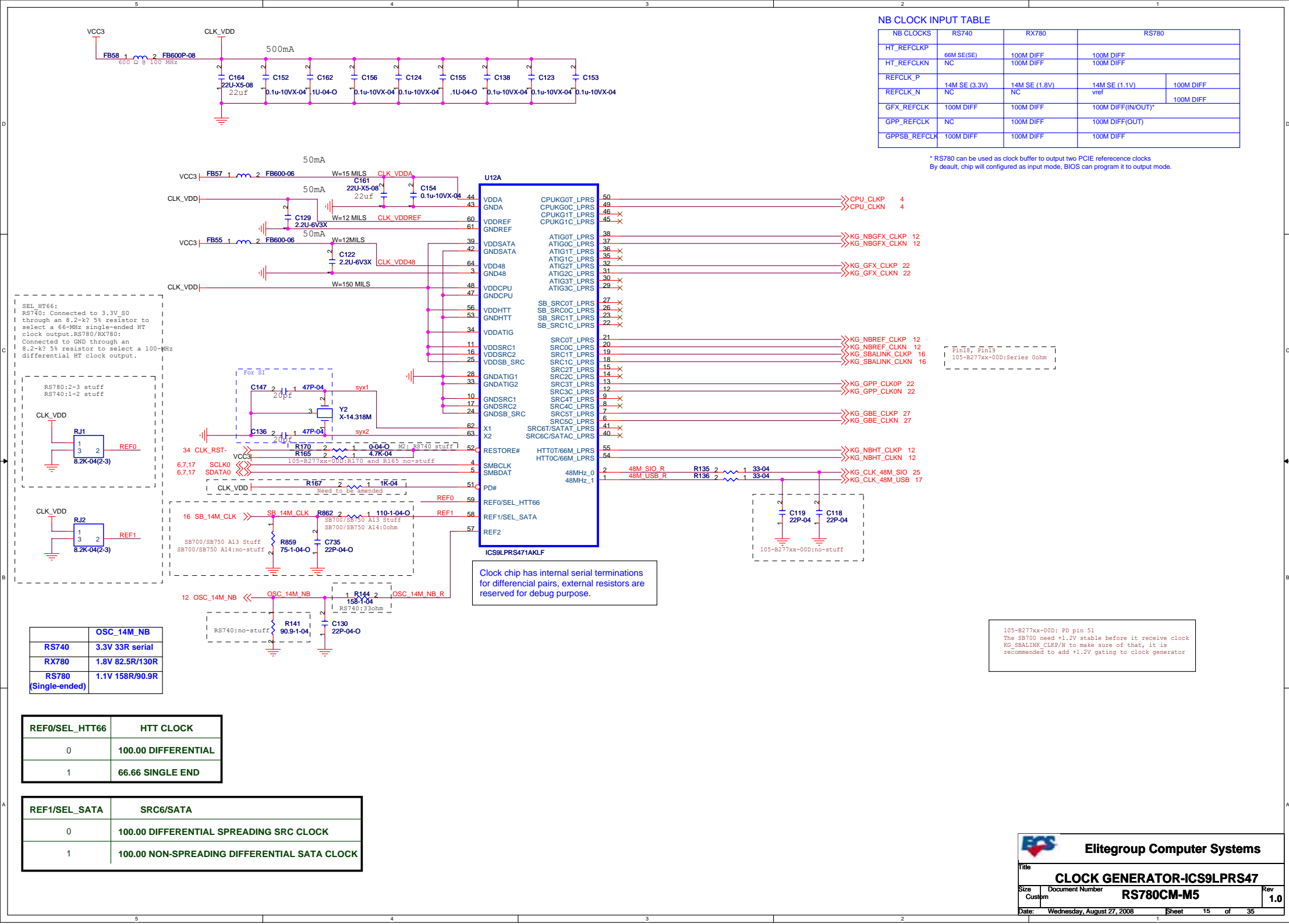


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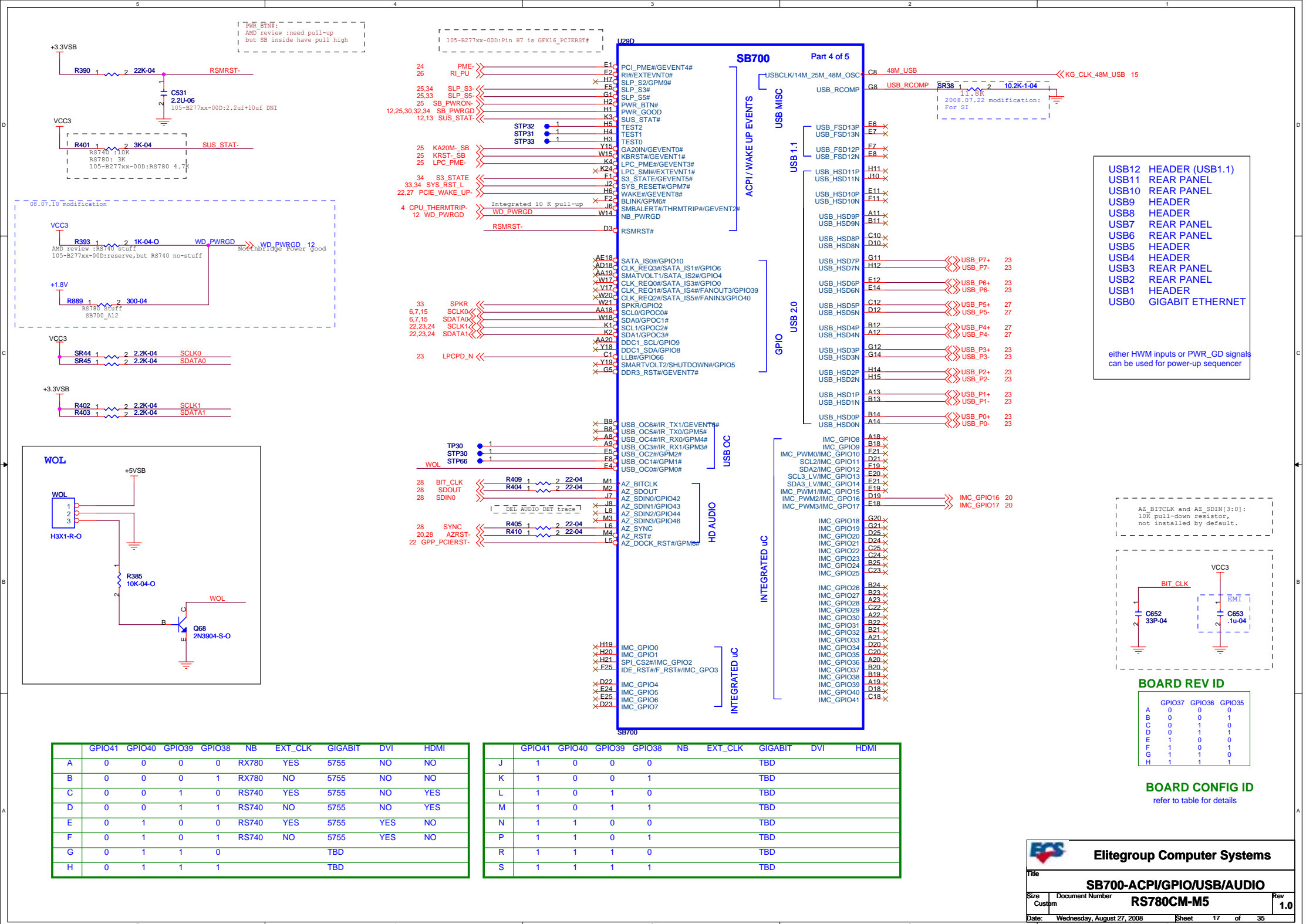
# NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

\* RS780 can be used as clock buffer to output two PCIe reference clocks  
By default, chip will configured as input mode, BIOS can program it to output mode.



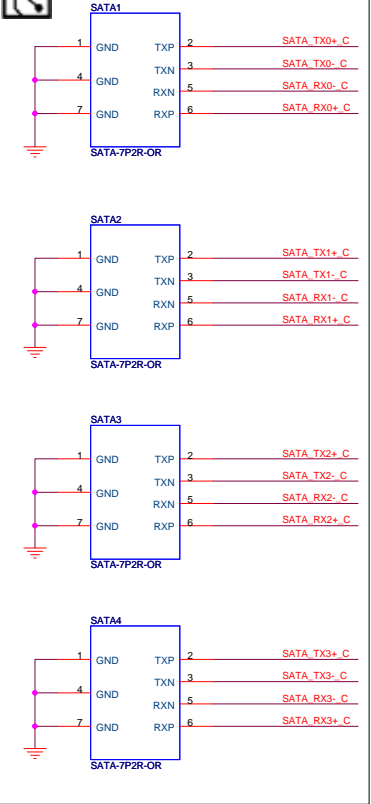




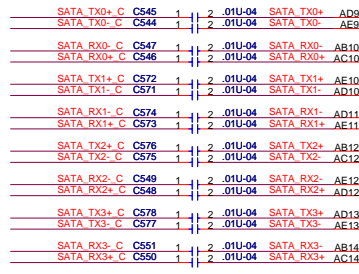


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Size	Document Number		Rev
Custom	<b>RS780CM-M5</b>		<b>1.0</b>
Date	Wednesday, August 27, 2008	Sheet	18 of 35

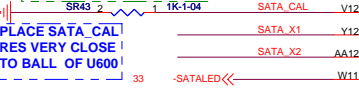
NOTE: J600&J601&J602&J603 ARE THT CONNECTORS



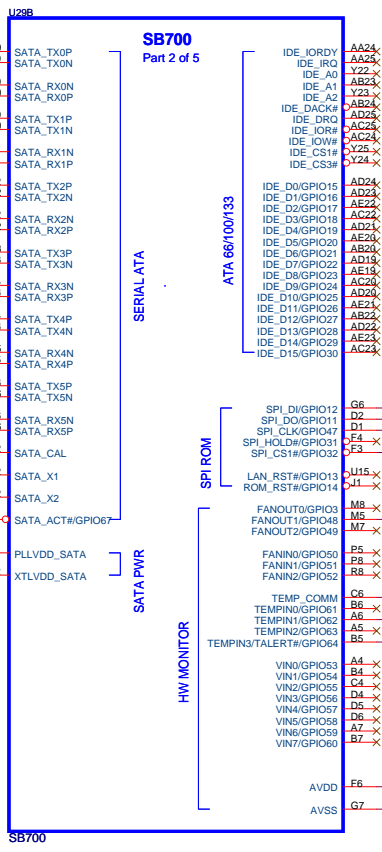
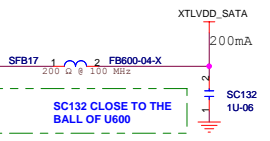
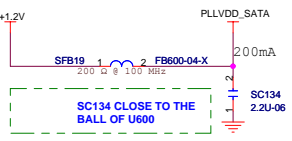
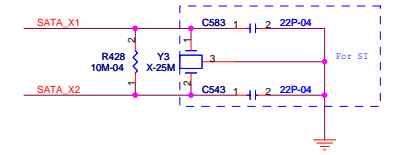
PLACE SATA AC COUPLING CAPS CLOSE TO SB600



NOTE: SR43 IS 1K 1% FOR 25MHZ XTAL, 4.99K 1% FOR 100MHZ INTERNAL CLOCK

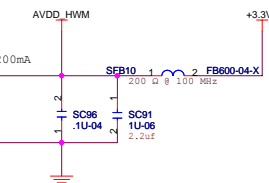
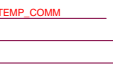
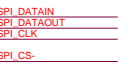
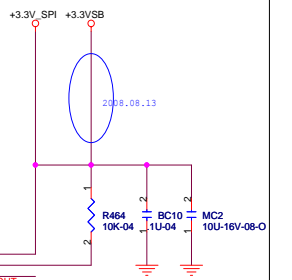
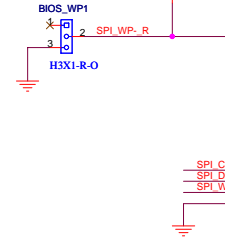


PLACE SATA\_CAL RES VERY CLOSE TO BALL OF U600

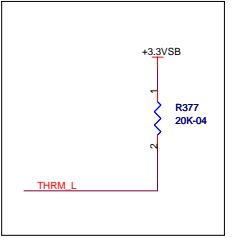


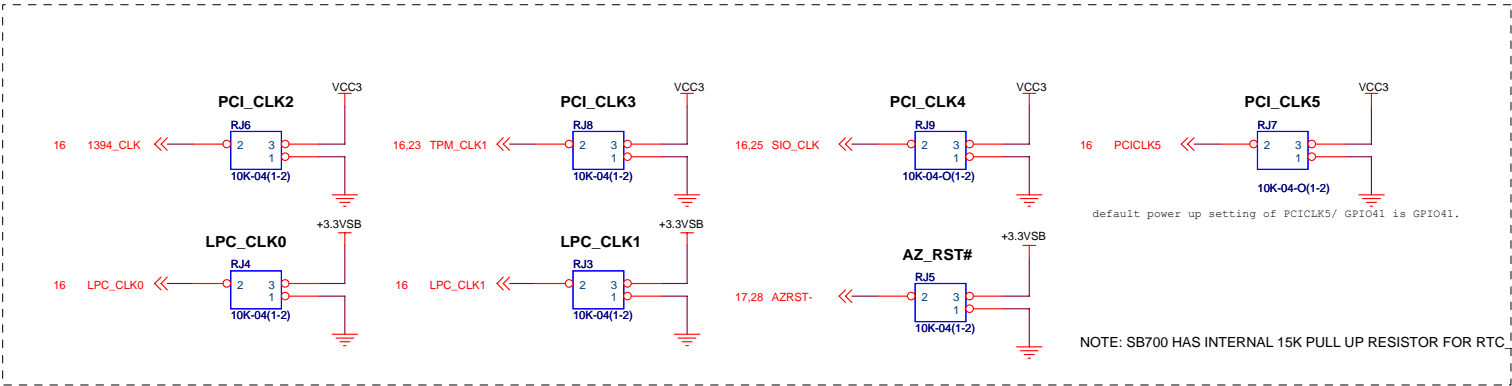
### DIP SPI ROM

BIOSWP	BIOS PROTECT
1-2	DISABLE
2-3	ENABLE



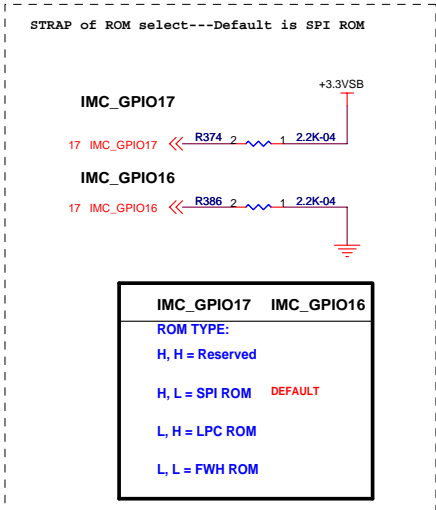
NOTE: ROUTE TEMP\_COMM AS A 10MIL TRACE





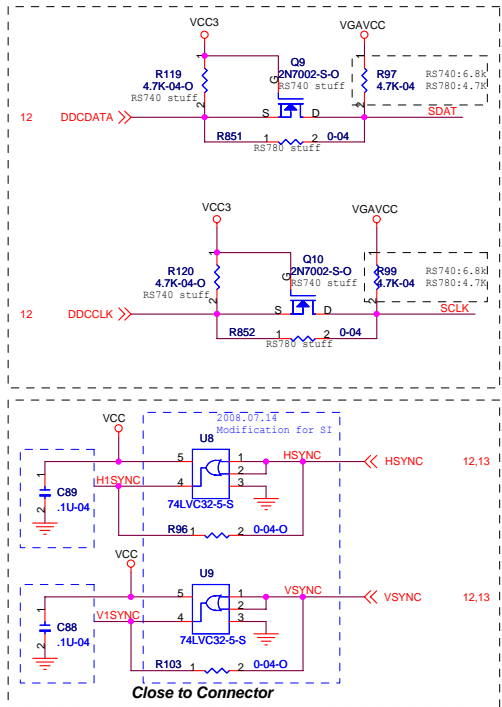
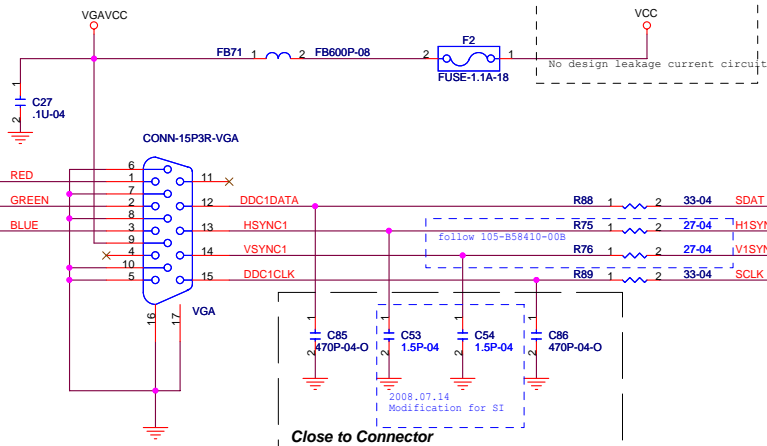
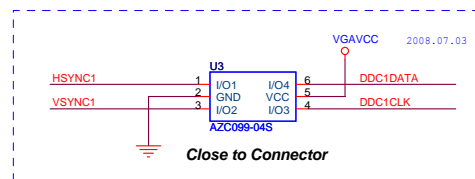
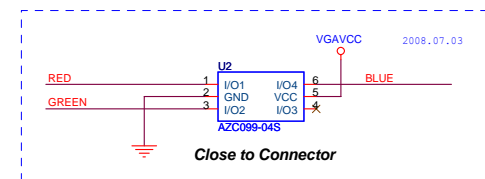
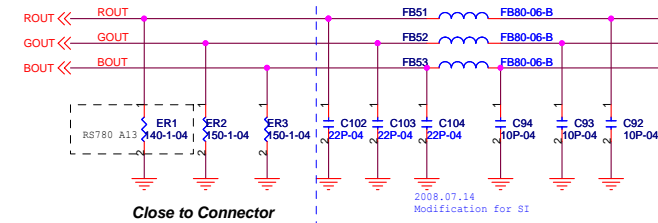
REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17	IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED	CLKGEN ENABLED	ENABLE PCI MEM BOOT	ROM TYPE: H, H = Reserved  H, L = SPI ROM    DEFAULT	
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	DISABLE PCI MEM BOOT DEFAULT	L, H = LPC ROM  L, L = FWH ROM	



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

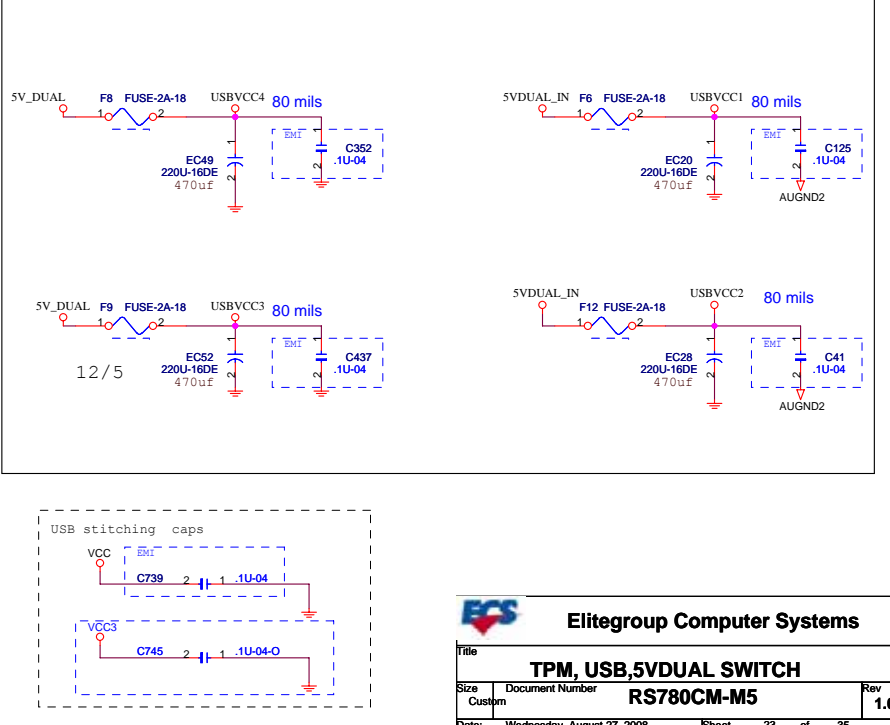
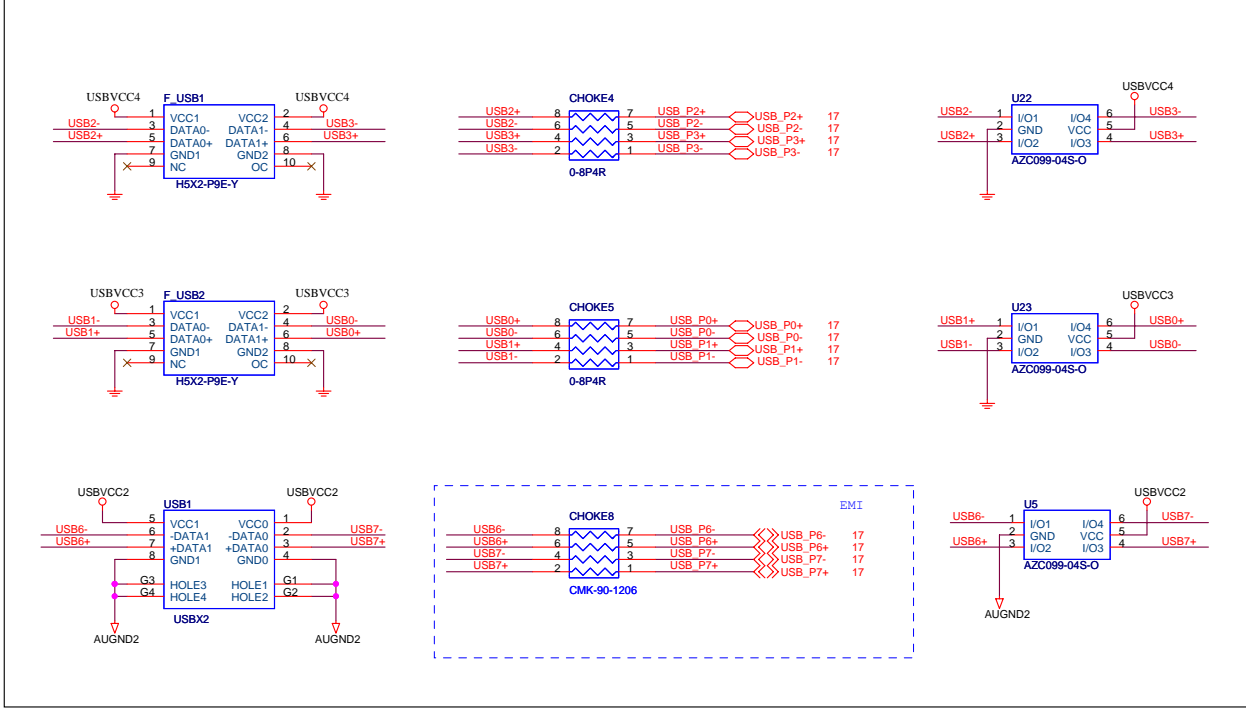
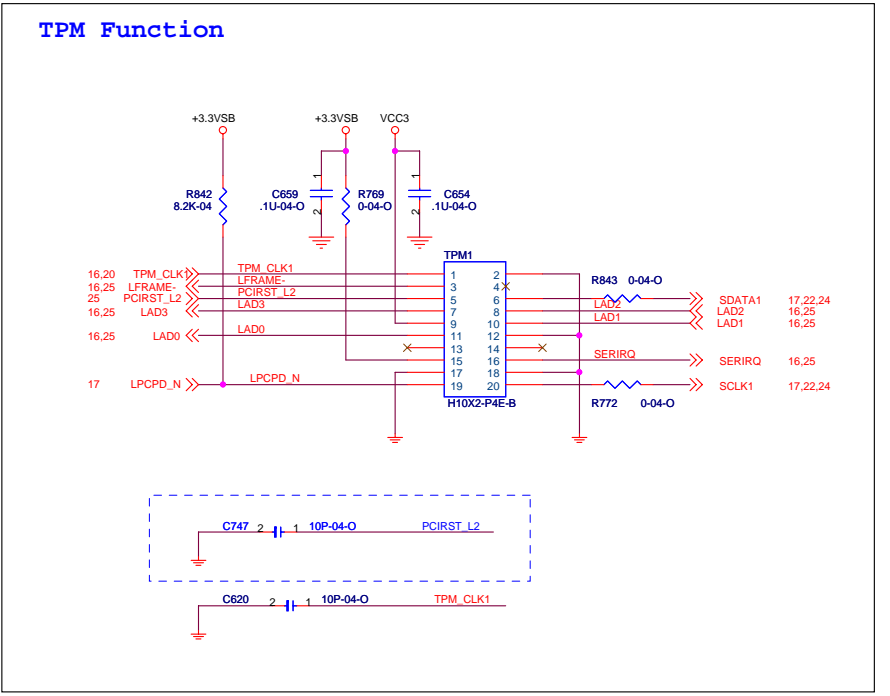
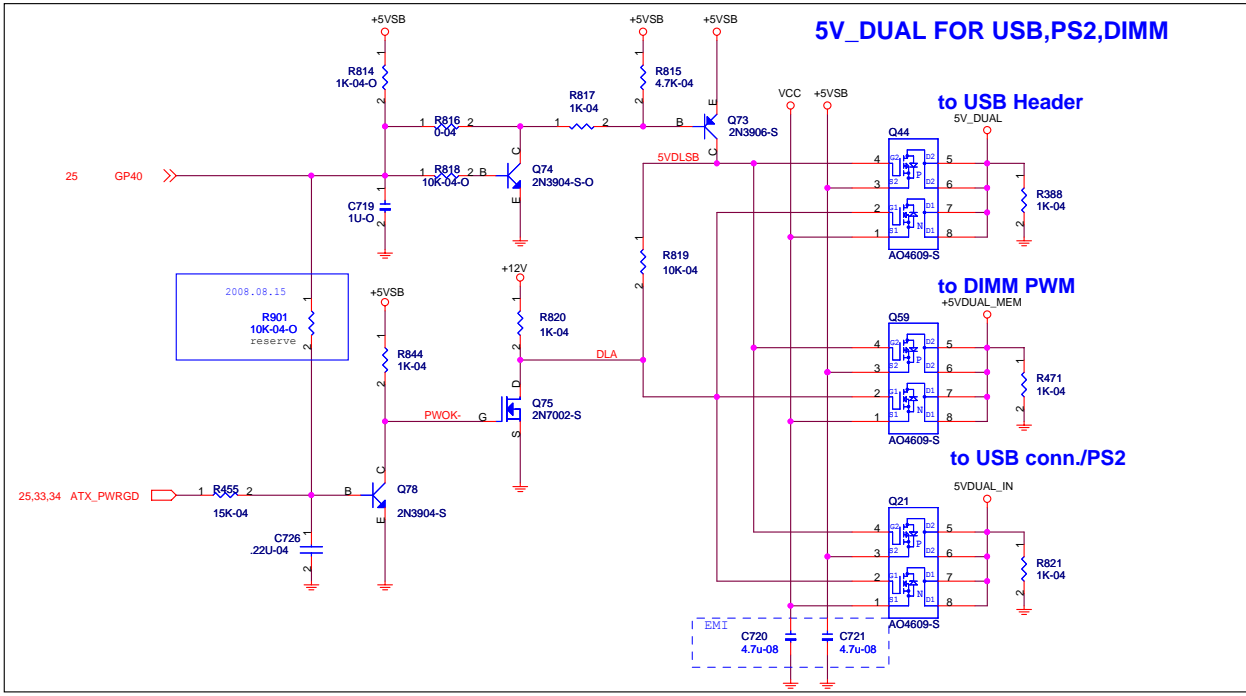
RS780 A13 \*:  
 • GREEN/BLUE: Connected to GND through two separate 150-? 1% resistors.  
 • RED: Connected to GND through two separate 140-? 1% resistors.



Elitegroup Computer Systems

Title		
CRT(D-sub)-VGA		
Size	Document Number	Rev
Custom	RS780CM-M5	1.0
Date:	Wednesday, August 27, 2008	Sheet 21 of 35

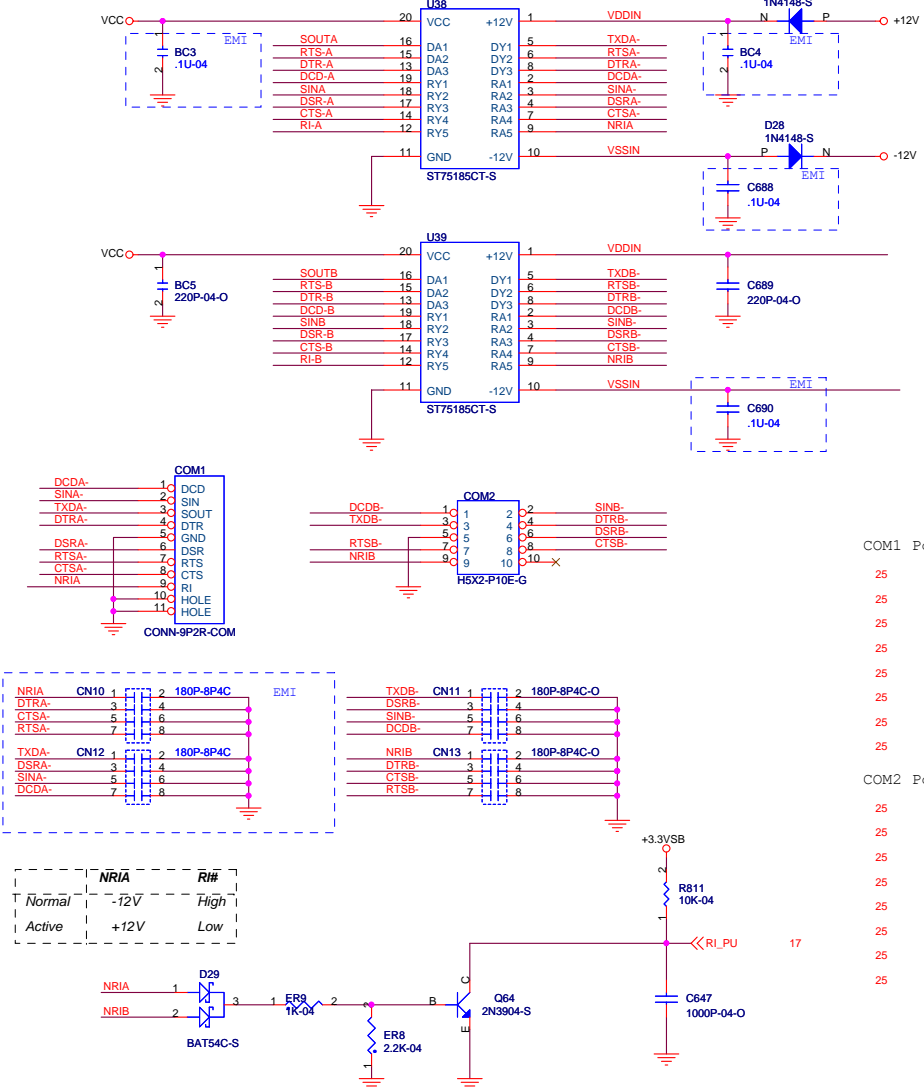




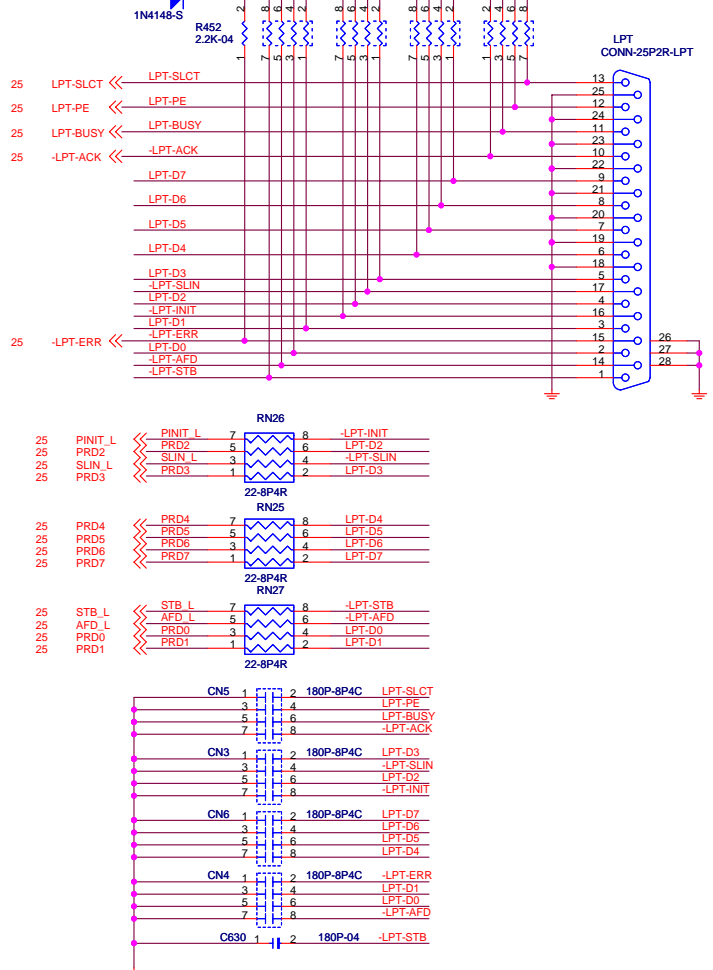




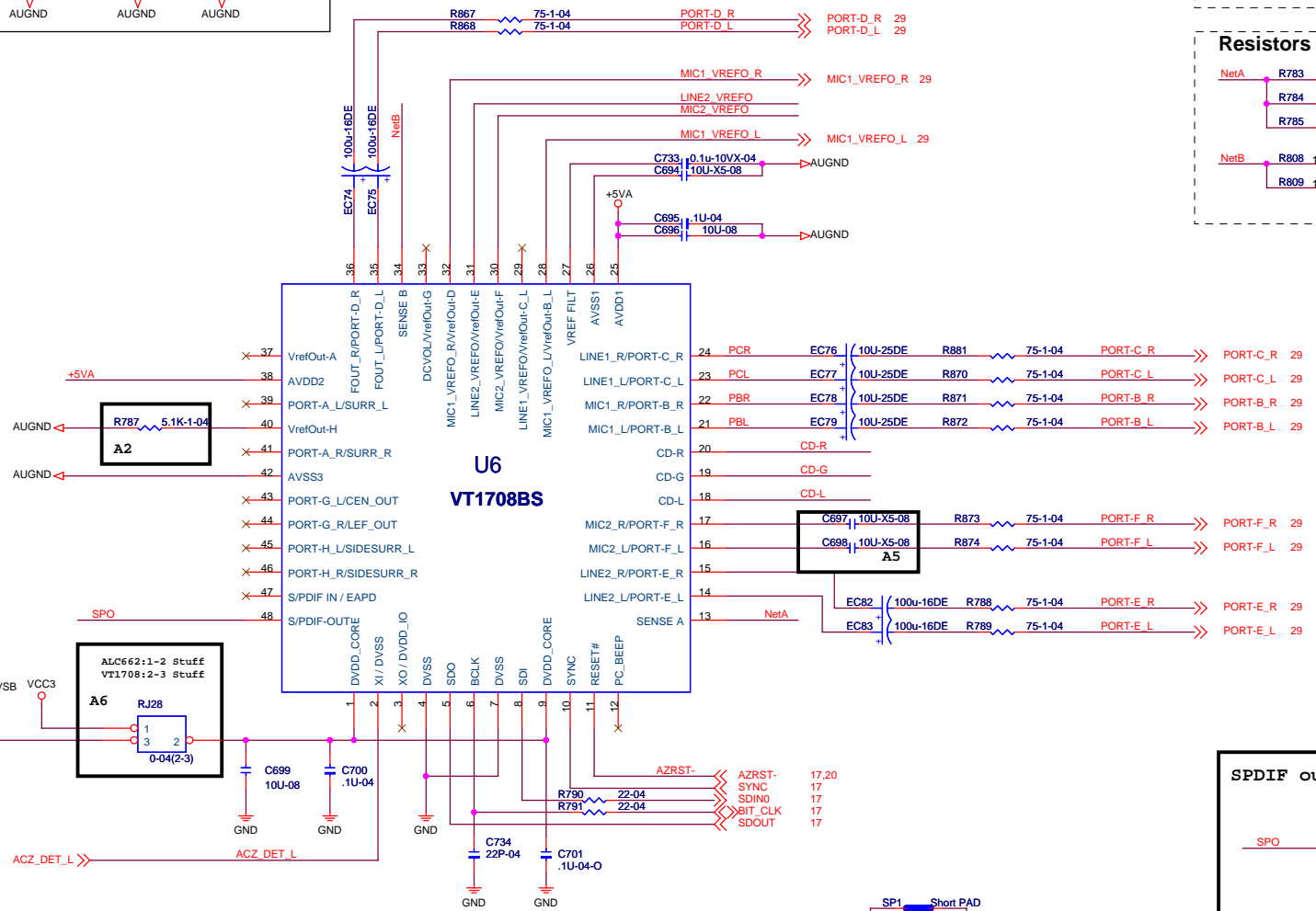
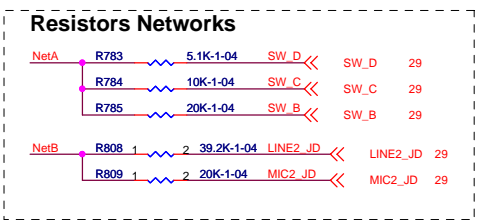
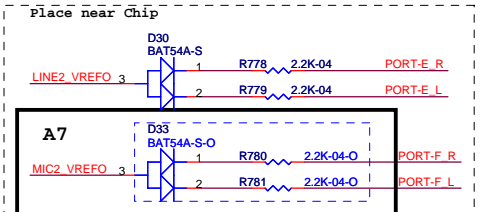
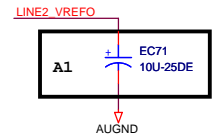
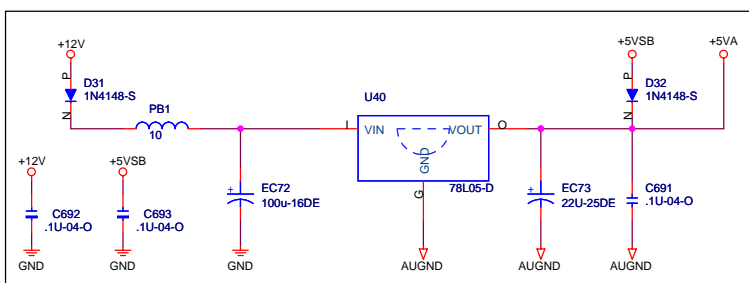
COM



LPT

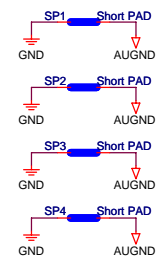
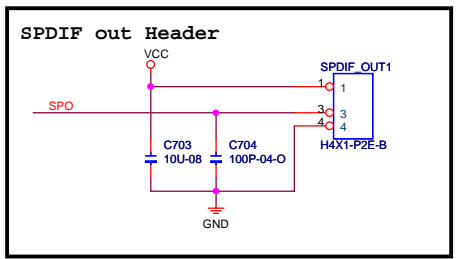
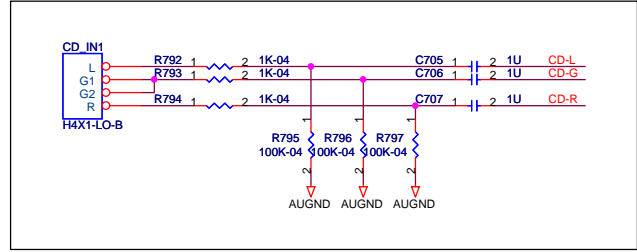


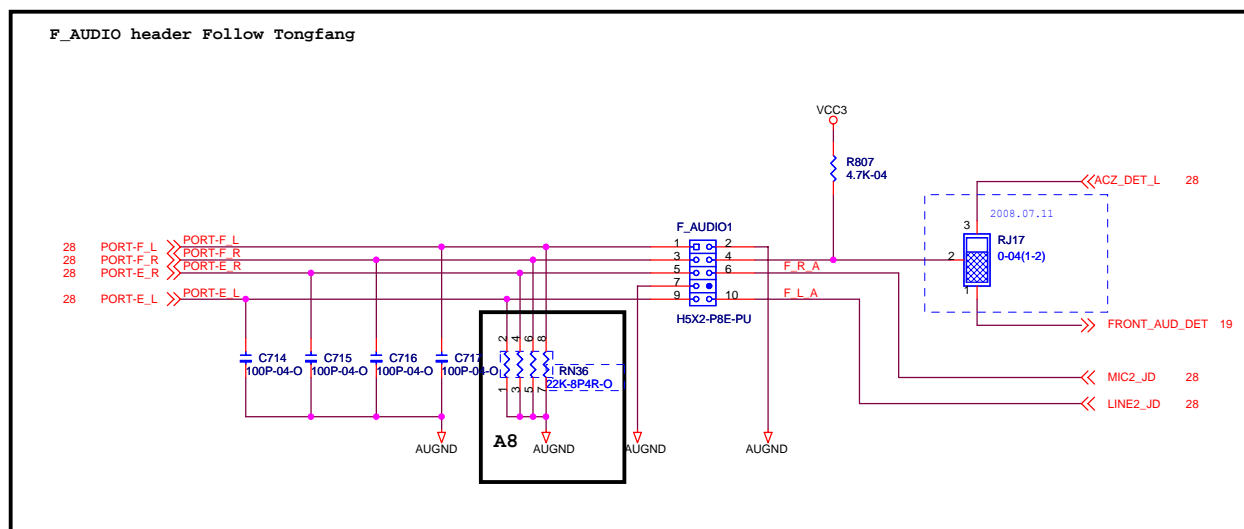
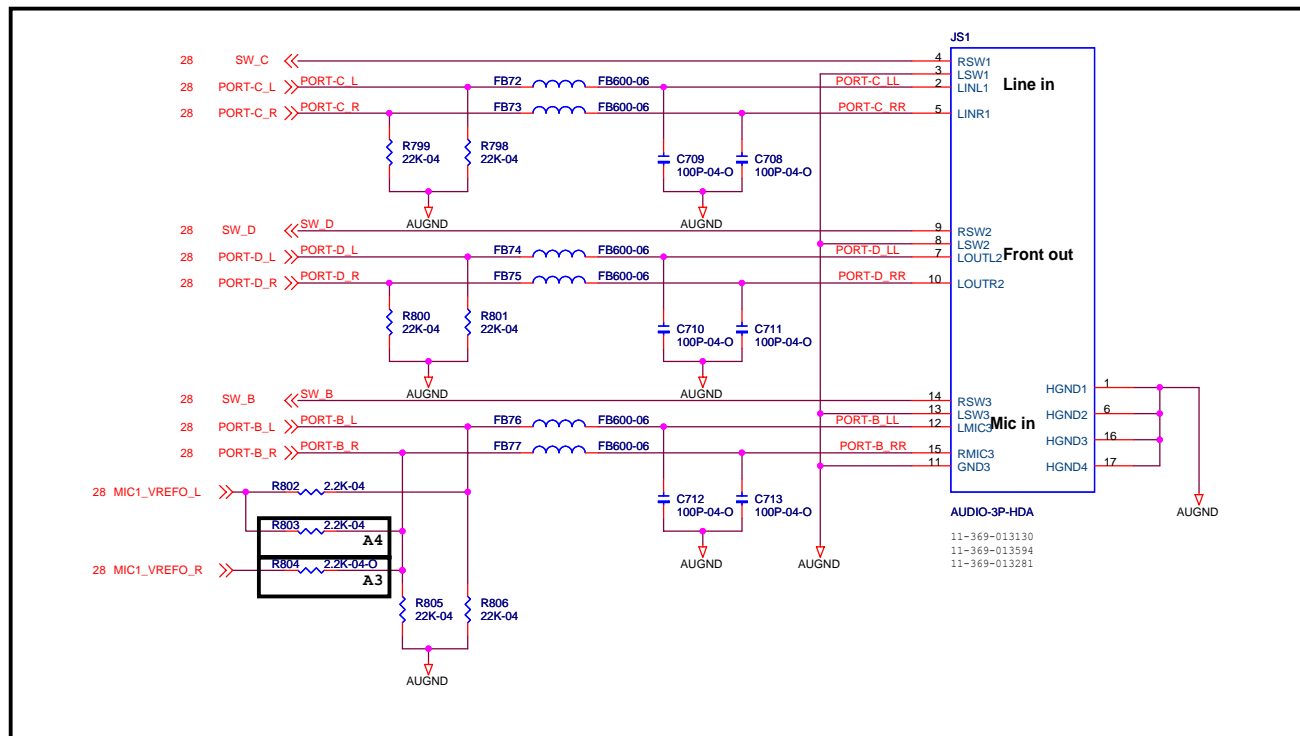




\*

	RT662VC	VT1708B
A1	NC	10U/25V
A2	20K-0402	5.1K-0402
A3	2.2K-0402	NC
A4	NC	2.2K-0402
A5	4.7U-08	10U-08
A6	VCC3	3VSB
A7	BAT54A-S	NC
A8	22K-8P4R	NC





Elitegroup Computer Systems

Title				
AUDIO VIA1708B/ALC662				
Size	Document Number			Rev
Custom	RS780CM-M5			1.0
Date:	Wednesday, August 27, 2008	Sheet	29	of 35

2008.07.14

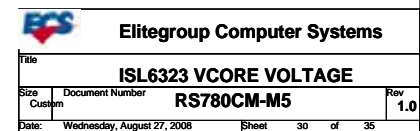
CO-layer RS740

CPU\_VDD\_RUN CPU\_VDDNB\_RUN

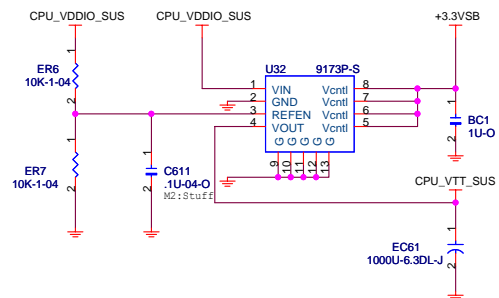
JW1 H2X1-0 RS740:stuff

CPU\_VDD\_RUN CPU\_VDDNB\_RUN

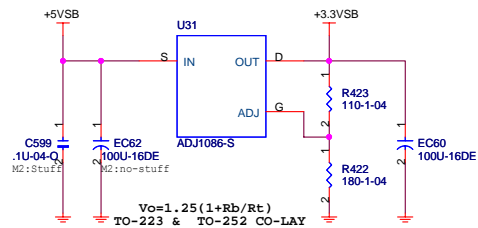
JW2 H2X1-0 RS740:reservation



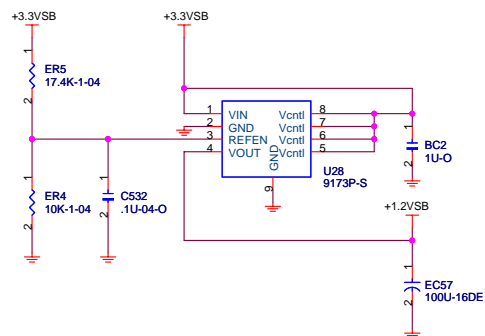
## DDRVTT



## 3VSB

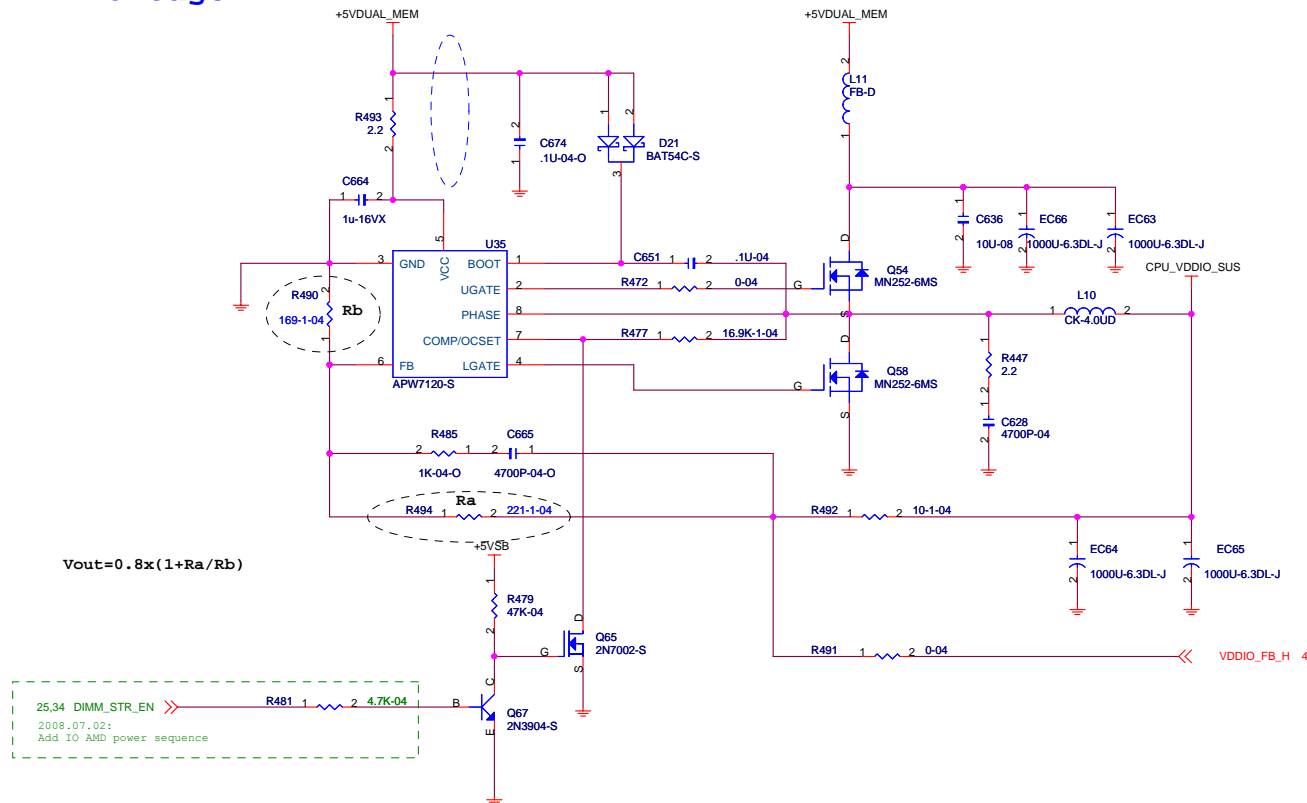


## 1.2VSB



## DDRII Voltage

$$V_{out} = 0.8 \times (1 + R_a/R_b)$$

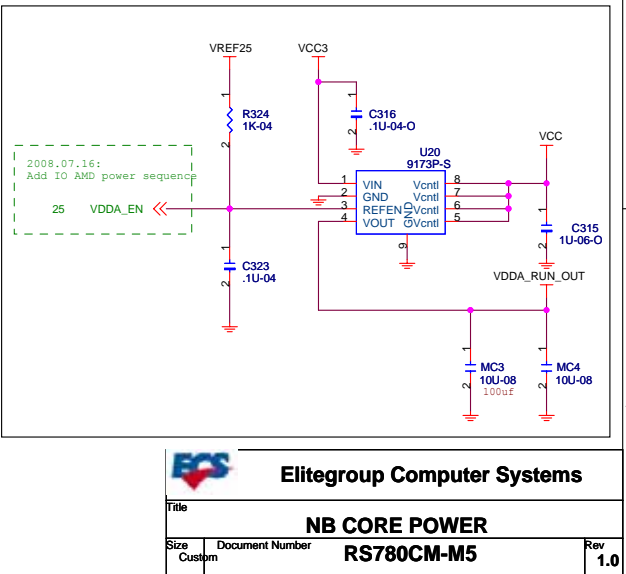
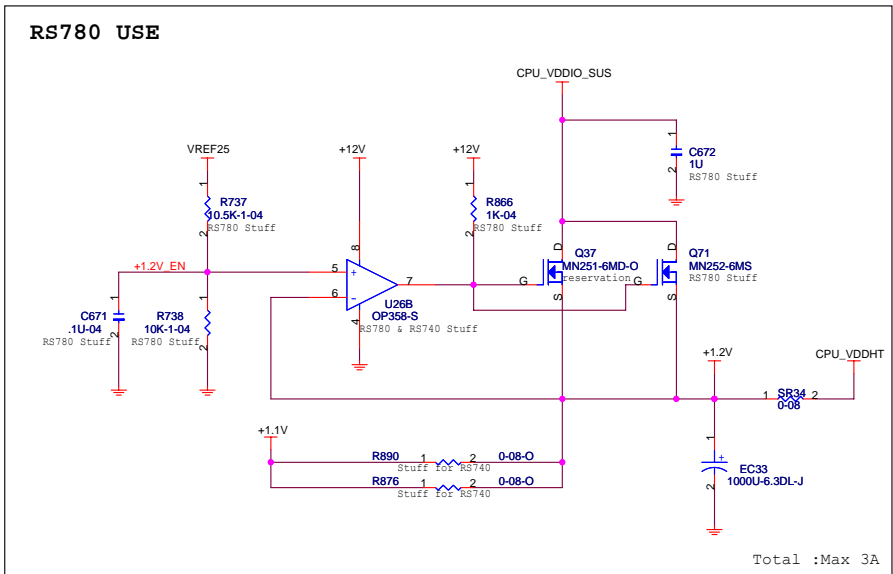
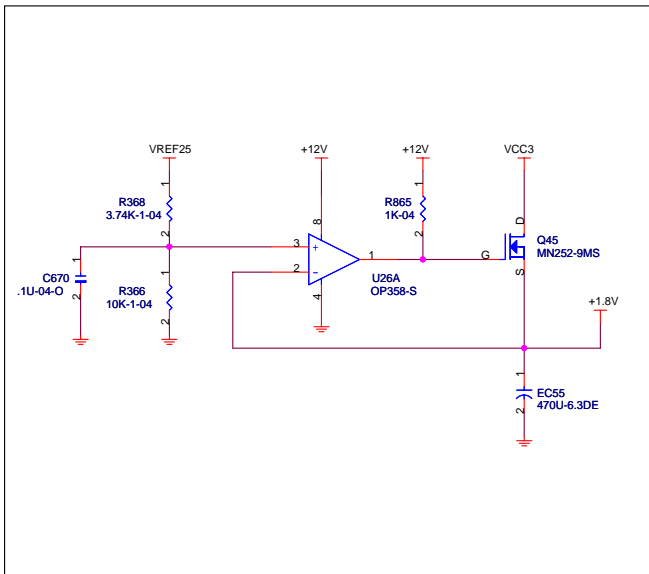
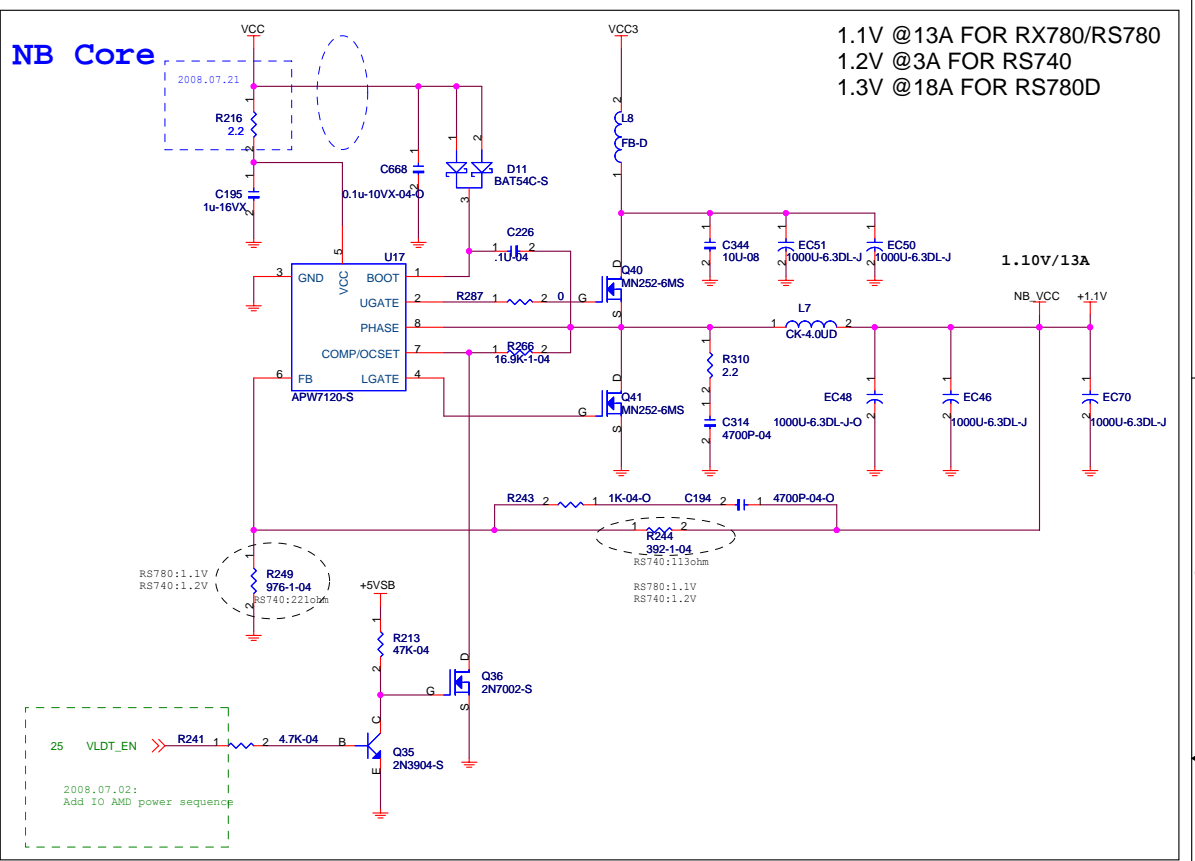
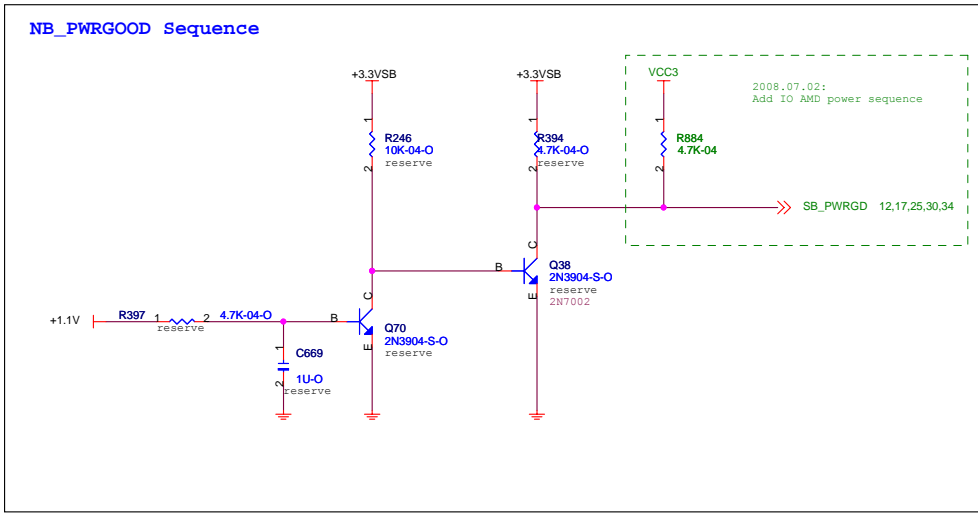
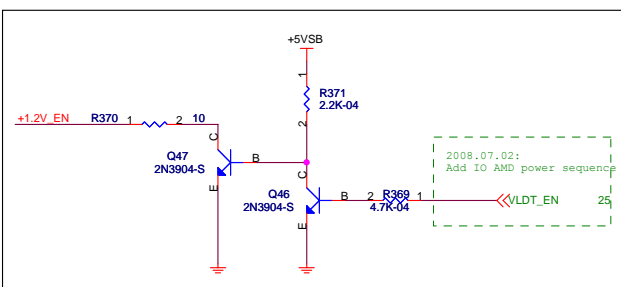
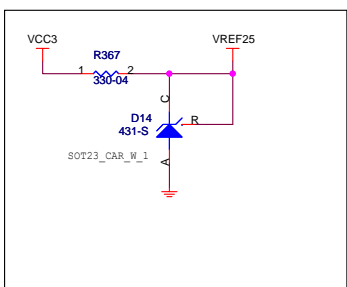


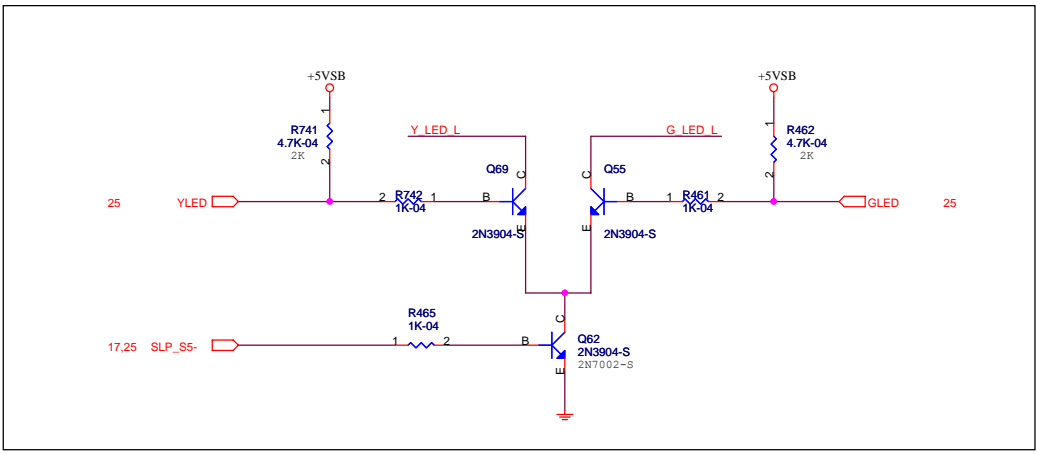
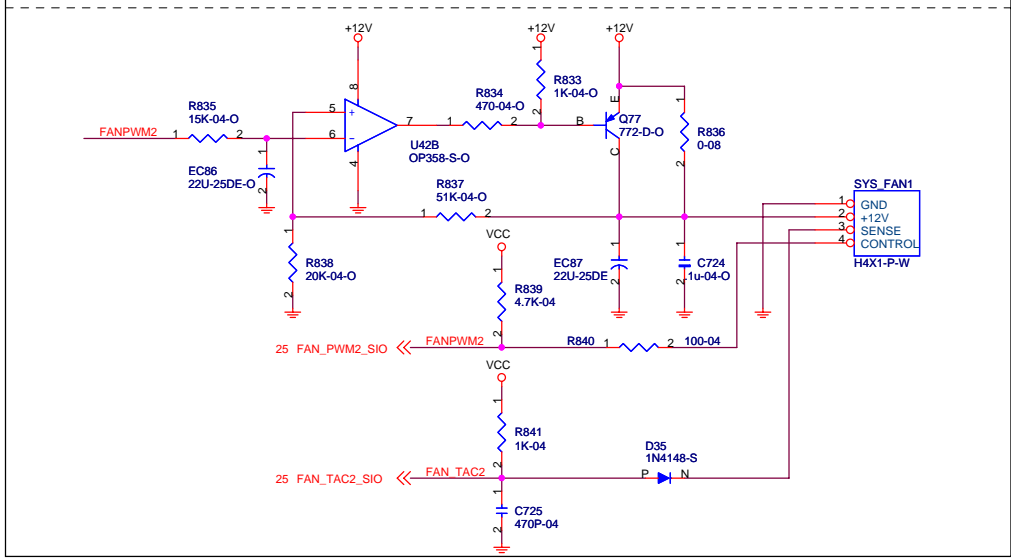
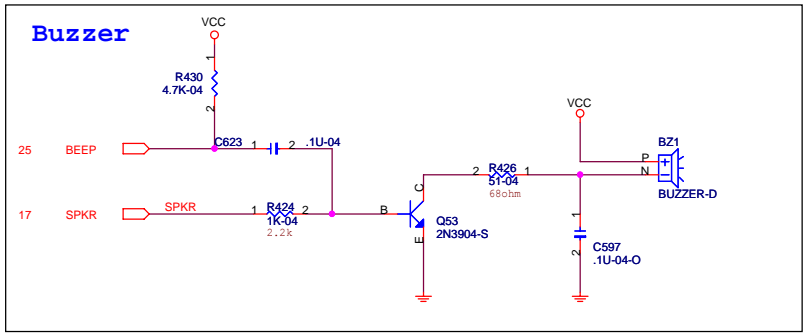
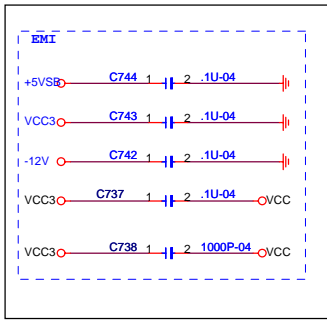
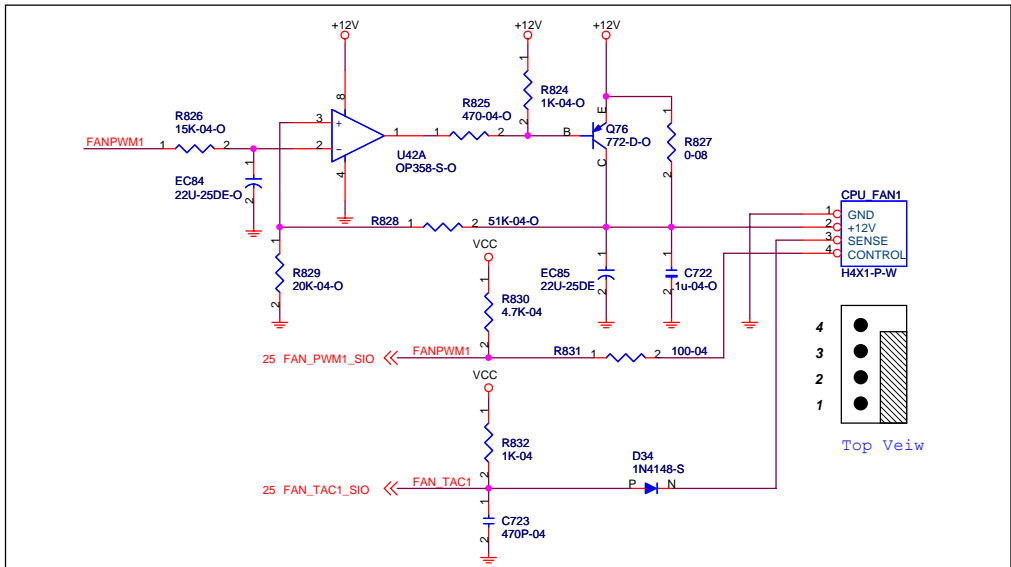
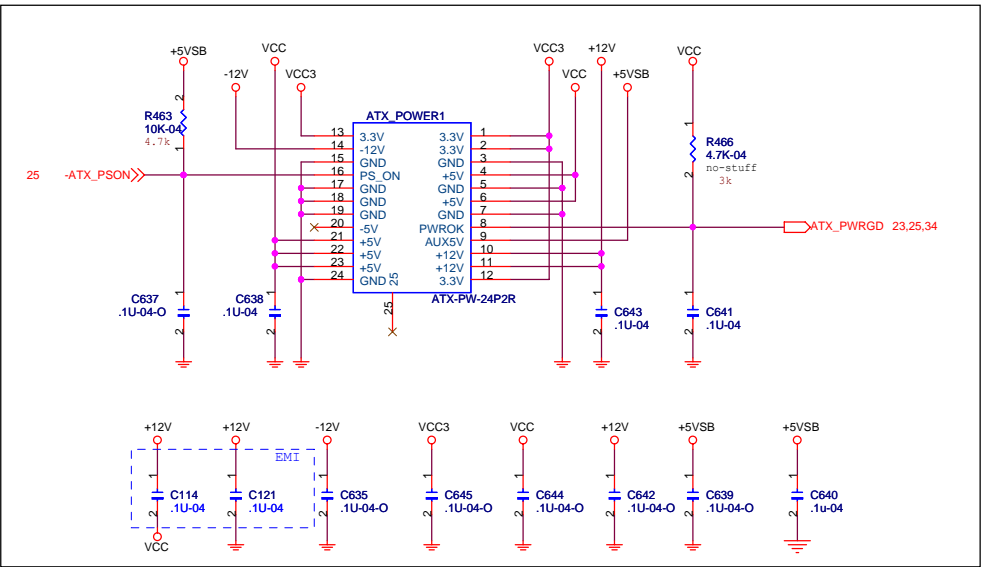
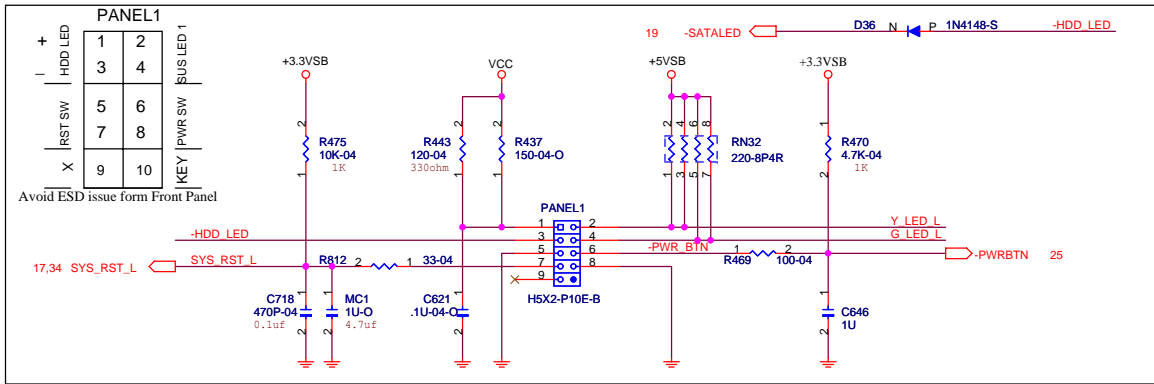
Del VDRAM\_PWRGD circuitry



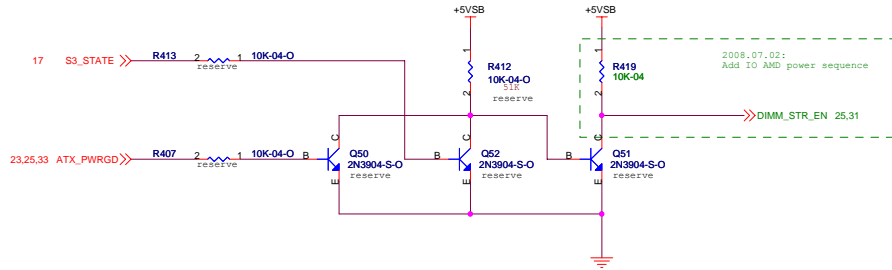
Elitegroup Computer Systems

Title			
DC POWER, DDRII POWER			
Size	Document Number		Rev
Custom	RS780CM-M5		1.0
Date:	Wednesday, August 27, 2008	Sheet	31 of 35

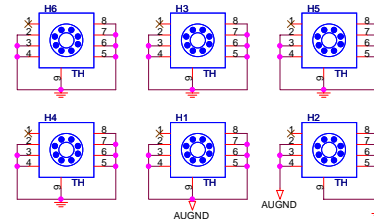
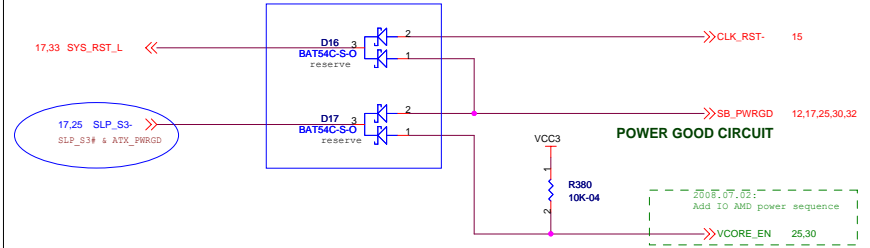




### ATHLON64 POWER GOOD & ENABLES CIRCUIT



### POWER GOOD & ENABLES



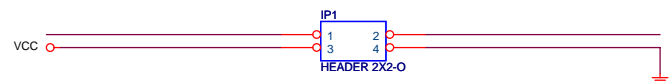
Elitegroup Computer Systems

Title		
POWER ENABLE		
Size	Document Number	Rev
Custom	RS780CM-M5	1.0
Date:	Wednesday, August 27, 2008	Sheet 34 of 35

NOTE:若為LAYOUT方便可改為兩個1X2 HEADER

不上件

CUPON



2116 : trace width 5 mil 60 ohm  
Trace Length 6096 mils  
Spacing: 1.clearance to itself 20/5/20(S:W:S)  
2.clearance to other signal 3W

1080 : trace width 4 mil 50 ohm  
Trace Length 6096 mils  
Spacing: 1.clearance to itself 50/4/50(S:W:S)  
2.clearance to other signal 3W

For 103

X2(wire)



For 104

SPI\_ROM\_D1(104)



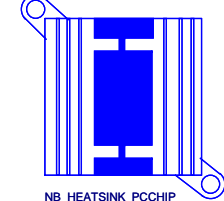
SPI-ROM-D-8M

BT1(104)



BATTERY

RS780(104)



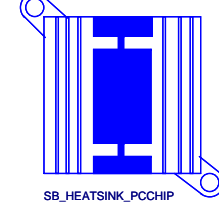
NB\_HEATSINK\_PCCHIP

CLR\_CMOS1(104)



JP-R-H

SB700(104)1



SB\_HEATSINK\_PCCHIP



Elitegroup Computer Systems

Title			Attention	
Size			Document Number	
Custom			RS780CM-M5	
Date:			Saturday, August 23, 2008	
Sheet			35 of 35	
Rev			1.0	